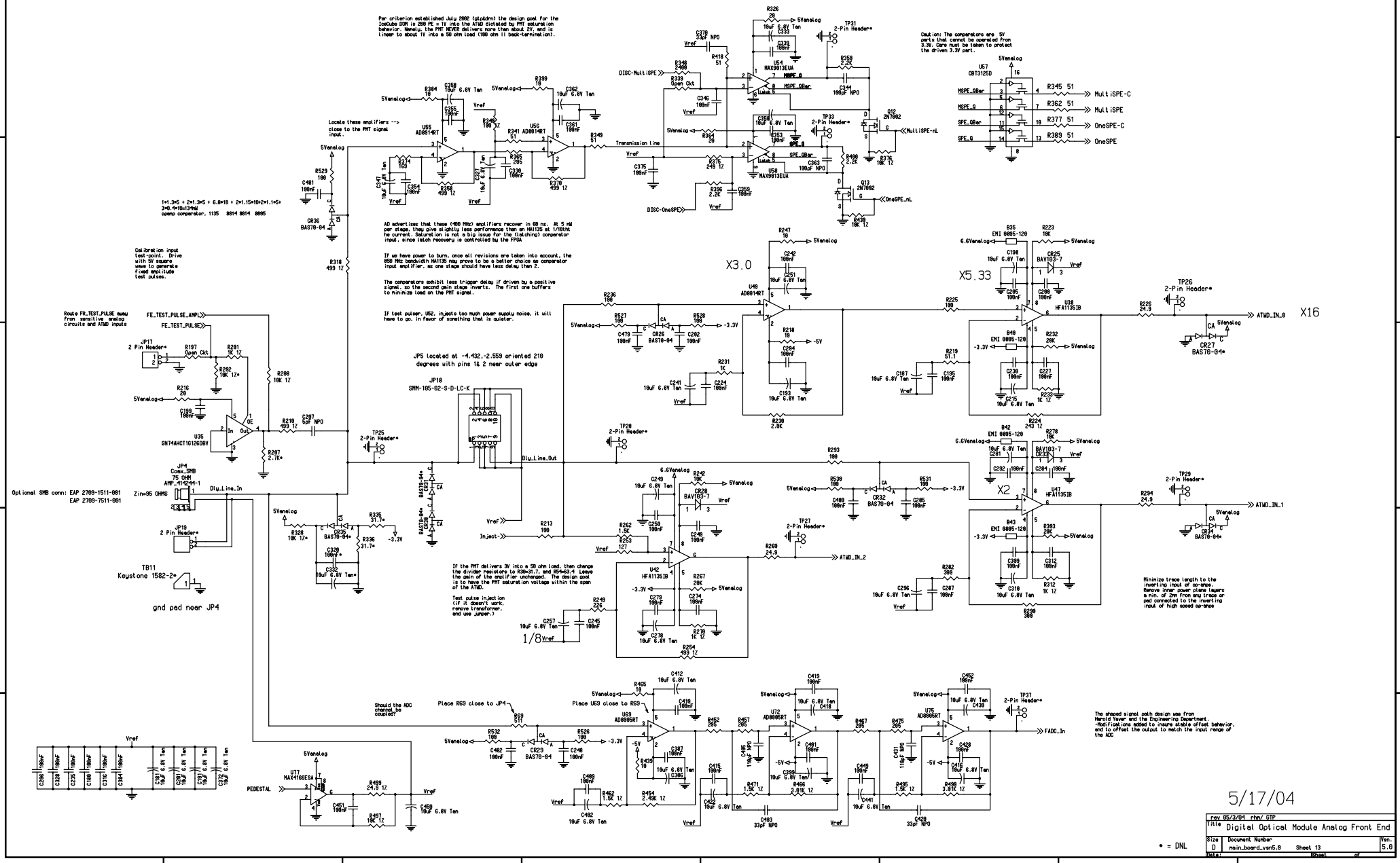
Per criterion established July 2002 (ptp&dm) the design goal for the IceCube DOM is 200 PE = 1V into the ATWD dictated by PMT saturation behavior. Namely, the PMT NEVER delivers more than about 2V, and is linear to about 1V into a 50 ohm load (100 ohm II back-termination).
Caution: The comparators are 5V parts that cannot be operated from 3.3V. Care must be taken to protect the driven 3.3V part.
Locate these amplifiers --> close to the PMT signal input.
AD advertises that these (400 MHz) amplifiers recover in 60 ns. At 5 mW per stage, they give slightly less performance than an HA1135 at 1/10tht he current. Saturation is not a big issue for the (latching) comparator input, since latch recovery is controlled by the FPGA
If we have power to burn, once all revisions are taken into account, the 850 MHz bandwidth HA1135 may prove to be a better choice as comparator input amplifier, as one stage should have less delay than 2.
The comparators exhibit less trigger delay if driven by a positive signal, so the second gain stage inverts. The first one buffers to mininize load on the PMT signal.
If test pulser, U52, injects too much power supply noise, it will have to go, in favor of something that is quieter.
Calibration input test-point. Drive with 5V square wave to generate fixed amplitude test pulses.
Route FR_TEST_PULSE away from sensitive analog circuits and ATWD inputs
JP5 located at -4.432,-2.559 oriented 210 degrees with pins 1& 2 near outer edge
Optional SMB conn: EAP 2709-1511-001 EAP 2709-7511-001
gnd pad near JP4
If the PMT delivers 3V into a 50 ohm load, then change the divider resistors to R38=31.7, and R54=63.4. Leave the gain of the amplifier unchanged. The design goal is to have the PMT saturation voltage within the span of the ATWD.
Test pulse injection (if it doesn't work, remove transformer, and use jumper.)
Minimize trace length to the inverting input of op-amps. Remove inner power plane layers a min. of 2mm from any trace or pad connected to the inverting input of high speed op-amps
The shaped signal path design was from Harold Yaver and the Engineering Department. -Modifications added to insure stable offset behavior, and to offset the output to match the input range of the ADC
Should the ADC channel be coupled?
Place R69 close to JP4
Place U69 close to R69
X3.0
X5.33
X2
X16
MultiSPE-C
MultiSPE
OneSPE-C
OneSPE
ATWD_IN_0
ATWD_IN_1
ATWD_IN_2
FADC_In
PEDESTAL
5/17/04
* = DNL
rev 05/3/04 rhn/ GTP
Title Digital Optical Module Analog Front End
Size D
Document Number main_board_vsn5.0
Sheet 13
Ven. 5.0
Date:
Sheet of