Board Stack-up:
TOP- Routing- Flud with ground plane where possible
Prepreg
INNER1 - Routing - controlled impedance pairs and general routing
Prepreg
GND - Power Plane
0.004" Prepreg
3.3V - Power Plane
Prepreg
INNER2 - Controlled Impedance and general routing
Prepreg
BOTTOM- Routing- Flood with copper where possible

Layout:
"Front" refers to the edge of the board to the right when looking at the component side of the board with PCI connector down.
Lay out LVDS pairs according to recommendations in Ch. 4 of http://www.national.com/appinfo/lvds/files/LOM_2.pdf.
Locate comparators and logic near front panel.
Locate DB-9 and LEMO connectors near each other.
Locate test connector at top (as close to top as reasonable),
Locate harmonica connector at back of board with openings facing up.
Space harmonica connector at least 1/2" down from top edge of board to allow for cable routing inside computer.
Locate LVDS drivers near harmonica connector.
MAKE LVDS PAIRS BETWEEN DRIVER AND HARMONICA CONNECTOR ALL THE SAME LENGTH!!!
Match lengths of + and - LVDS lines in pairs. (see reference)
Jumper footprints and open-ckt footprints should be the same size to permit easy configuration change.

Build:
Both Y1 and Y2 cannot be mounted at the same time.

Rev B Changes
1) change R63 to open circuit, Change C40 (from JP3 to U13-2) to R119 = 4.7K.
2) R66 & R68 pads to 1210 size.
3) Suggest change 1uF Capacitors, C18, C23, C24, C27, C36, C38, C44, C45, C50, C58, C61, C63, C65, C67, C68, C72 and C74, to X7R Ceramic (DC020703FIF) 0805 size
4) R26, R27, R32 to 511ohm 0805.
5) S1 connect only to pin 1, pin2, the switch contacts.
6) Change regulator, U2, to National Semiconductor LP3964 EMP-3.3
7) Add fuses F1, F2, F3
8) Add provisional loading instructions to build instructions to loading house.
9) Change Y1 footprint. Three of 5 pads out of position.
10) Add four protective diodes, D9, D10, D11 and D12.
11) Add ground pins on JP3 (RJ45 input connector)
12) Add ground pins on JP2A and JP2B
13) Change DS1, DS2, DS3 to a three-in-one verticle LED unit DS1a,b,c.
14) Add feature for using modem control lines to generate sync pulse.
15) Revise end panel layout to accommodate LED change. Allow for access to S1 from rear panel.
16) Shorten board by 1/16" (?)

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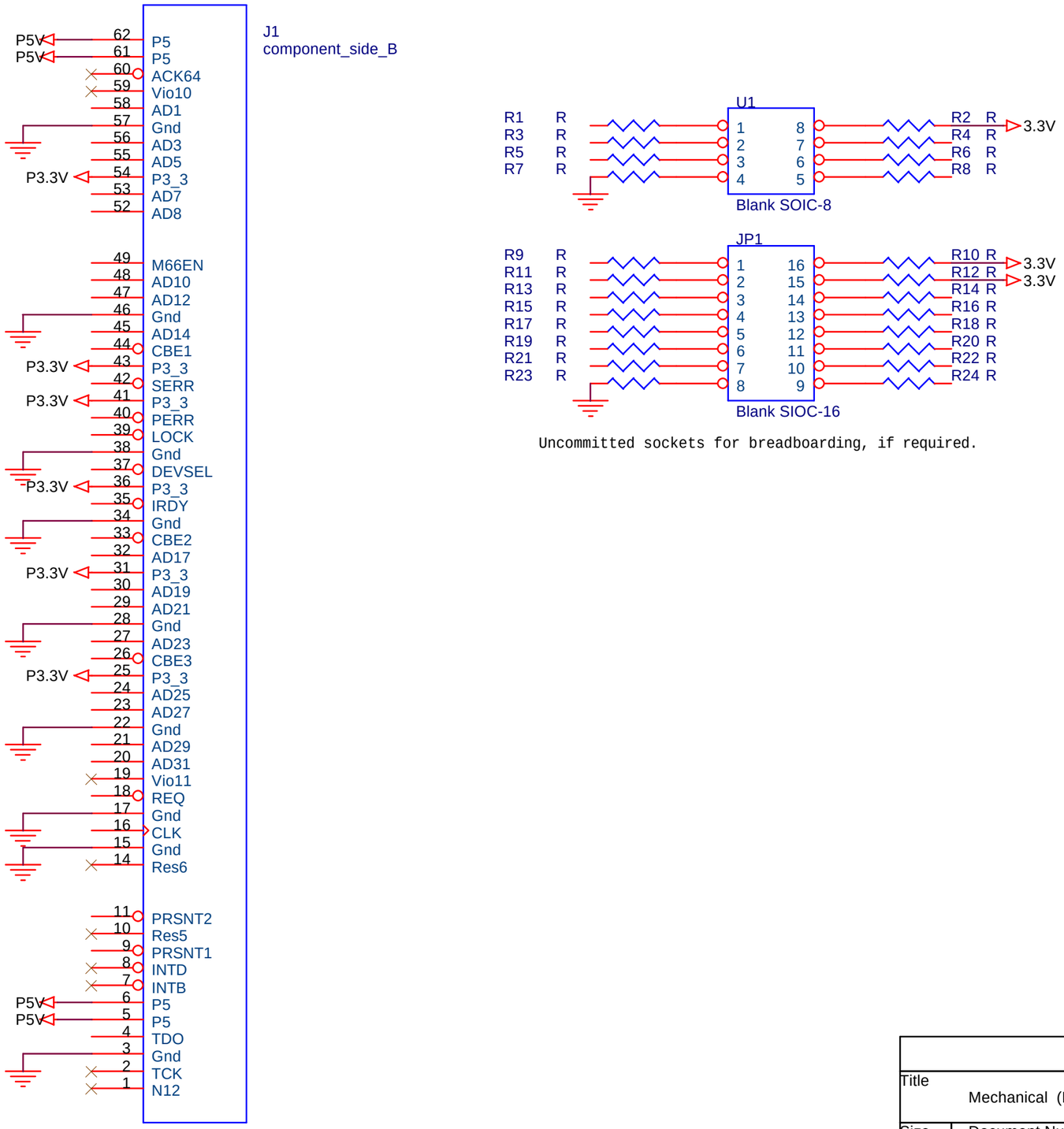
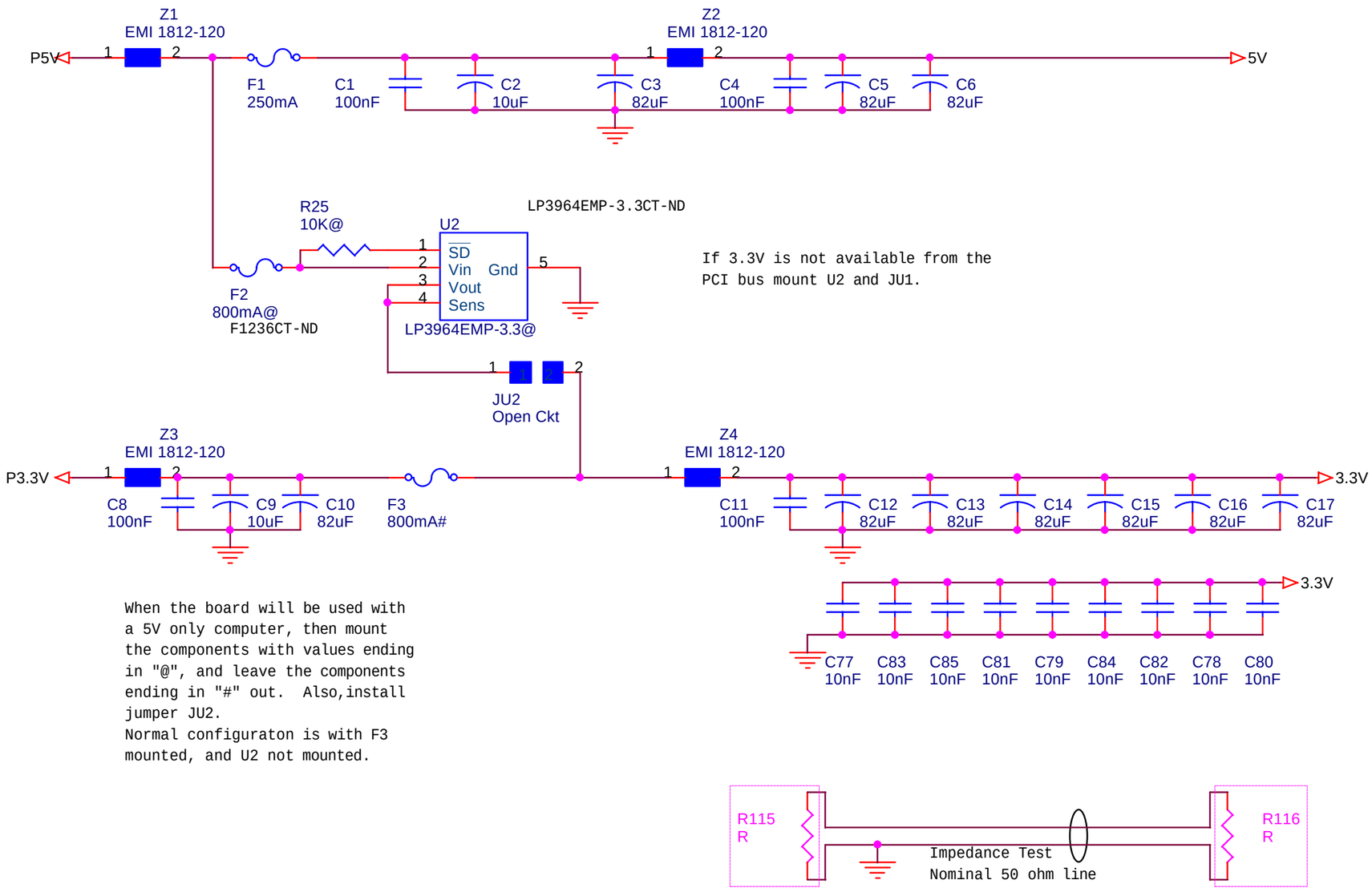
Title	Fabrication (Rev B 7/7/04)	
Size A	Document Number DSB-Sheet1	Rev A
Date: Friday, July 09, 2004	Sheet 1 of 4	



Uncommitted sockets for breadboarding, if required.

Title	Mechanical (Rev B 7/7/04)	
Size A	Document Number DSB-Sheet2	Rev A
Date: Friday, July 09, 2004	Sheet 2 of 4	



If 3.3V is not available from the PCI bus mount U2 and JU1.

When the board will be used with a 5V only computer, then mount the components with values ending in "@", and leave the components ending in "#" out. Also,install jumper JU2.
Normal configuraton is with F3 mounted, and U2 not mounted.

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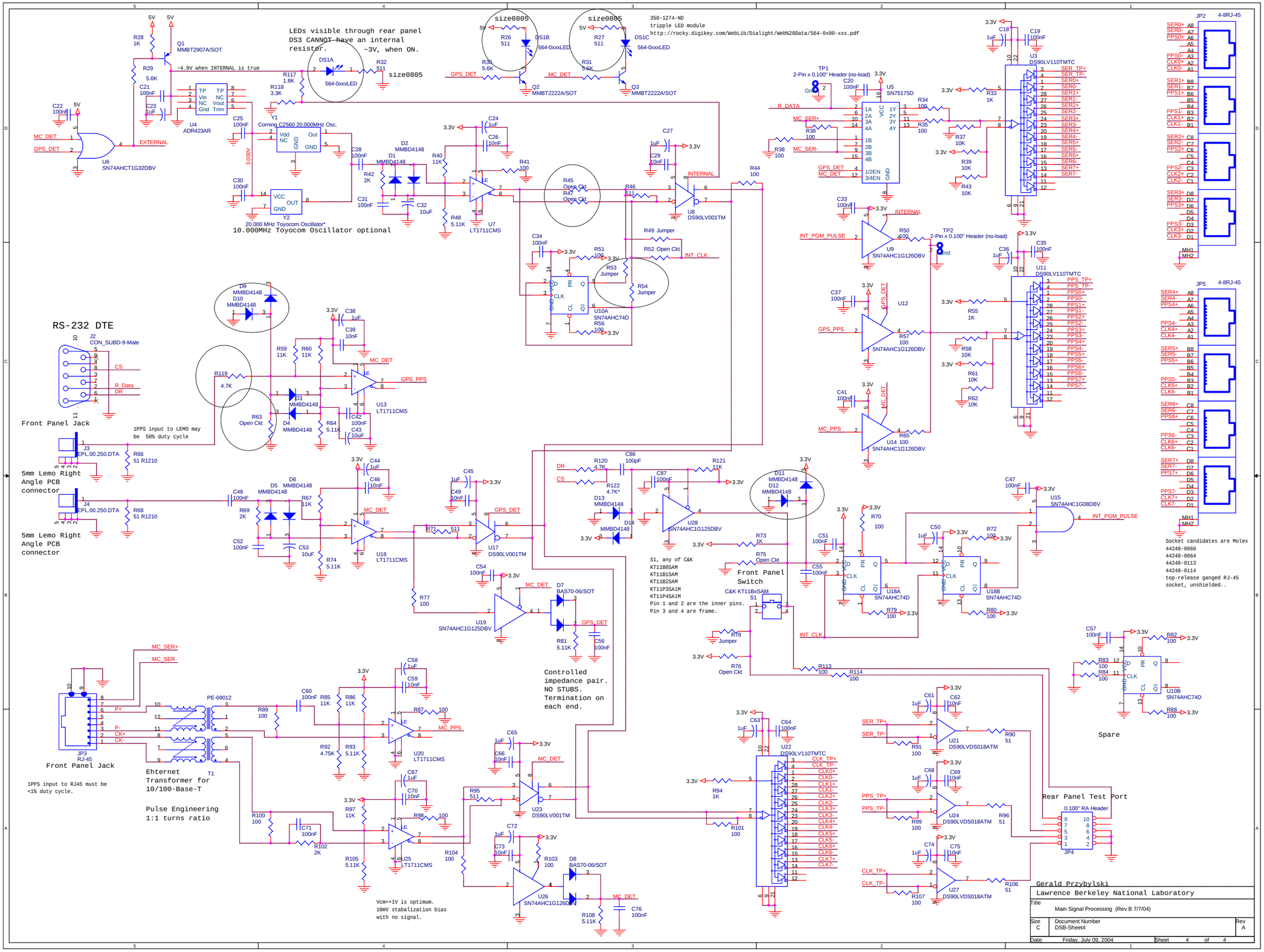
Title	Power (Rev B 7/7/04)	
Size A	Document Number DSB-Sheet 3	Rev A
Date: Friday, July 09, 2004	Sheet 3 of 4	


LEDs visible through rear panel
DS3 CANNOT have an internal
resistor. ~3V, when ON.
350-1274-ND
trippple LED module
http://rocky.digikey.com/WebLib/Dialight/Web%20Data/564-0x00-xxx.pdf
~4.9V when INTERNAL is true
Coming C2560 20.000MHz Osc.
20.000 MHz Toyocom Oscillator*
10.000MHz Toyocom Oscillator optional
RS-232 DTE
Front Panel Jack
1PPS input to LEMO may
be 50% duty cycle
5mm Lemo Right
Angle PCB
connector
Front Panel Jack
1PPS input to RJ45 must be
<1% duty cycle.
Ehternet
Transformer for
10/100-Base-T
Pulse Engineering
1:1 turns ratio
Vcm=+1V is optimum.
10mV stabalization bias
with no signal.
Controlled
impedance pair.
NO STUBS.
Termination on
each end.
S1, any of C&K
KT11B0SAM
KT11B1SAM
KT11B2SAM
KT11P3SA1M
KT11P4SA1M
Pin 1 and 2 are the inner pins.
Pin 3 and 4 are frame.
Front Panel
Switch
C&K KT11BxSAM
Socket candidates are Molex
44248-0060
44248-0064
44248-0113
44248-0114
top-release ganged RJ-45
socket, unshielded..
Spare
Rear Panel Test Port
0.100" RA Header
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Title
Main Signal Processing (Rev B 7/7/04)
Size C
Document Number DSB-Sheet4
Rev A
Date: Friday, July 09, 2004
Sheet 4 of 4