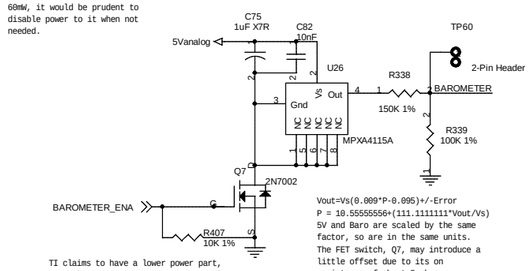
Since the sensor uses about 60mW, it would be prudent to disable power to it when not needed.

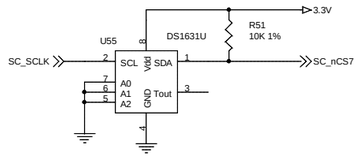


TI claims to have a lower power part, but only accurate to 2 deg C (probably within the -25C and above range)...

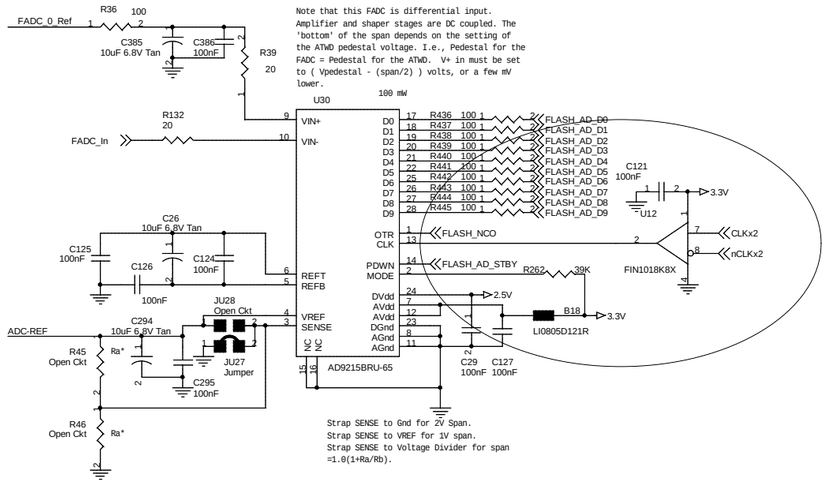
Vout=Vs(0.009*P-0.095)+/-Error
P = 10.55555556+(111.1111111*Vout/Vs)
5V and Baro are scaled by the same factor, so are in the same units.
The FET switch, Q7, may introduce a little offset due to its on resistance of about 5 ohms.

-(-5/2.5)-(+3.3+2.5+1.8)/4 =Vout
2 - 0.825 - 0.625 - 0.450) = 0.100V
Lets just assume that if +5 is gone, we're dead. The 5V CPU supervisory chip input will cause reboot below about 4.750V.

Part values ending in "*" should not be mounted. These parts are for diagnostics or implementation of alternate methodologies.

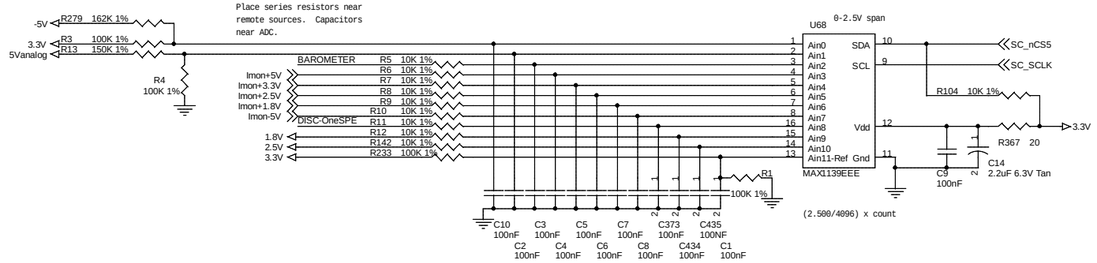


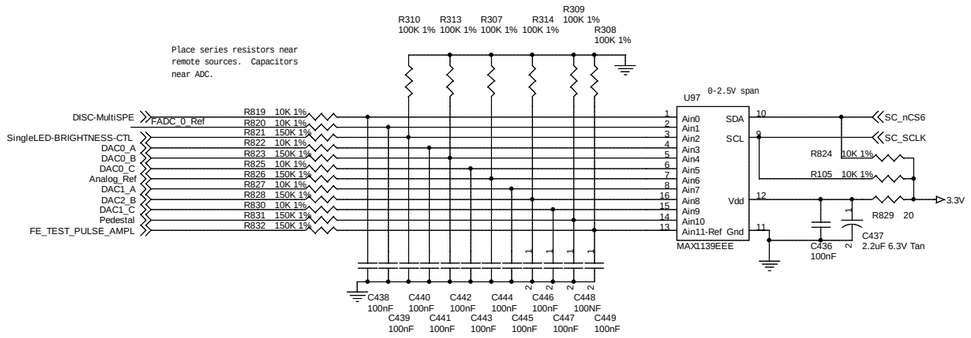
4.25 mW x 4 + 7.5mW = 24.5 mW
plus 3.3mW when converting temperature
+ 6mW x 10V/conv_eff = 67 mW

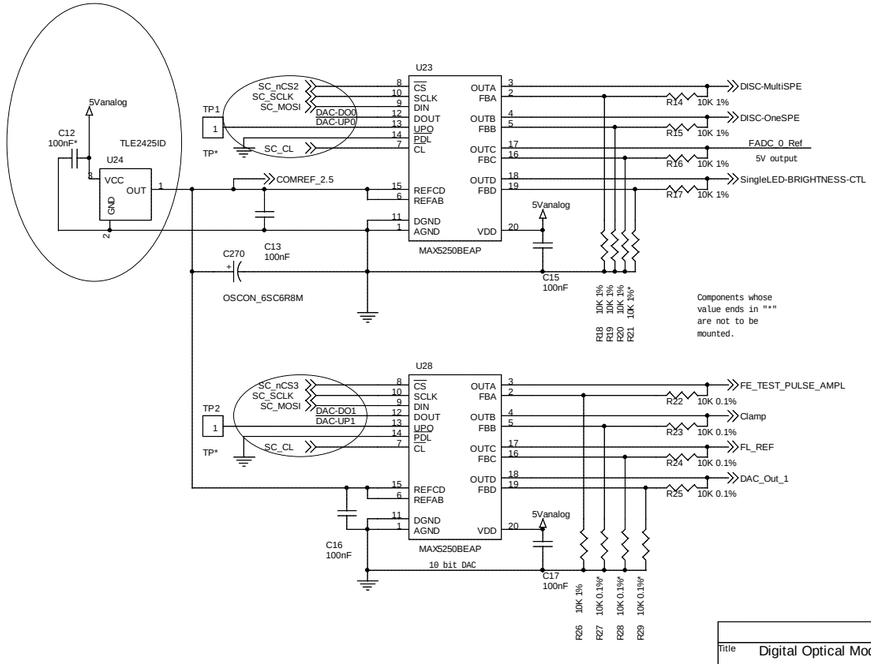


Note that this FADC is differential input. Amplifier and shaper stages are DC coupled. The 'bottom' of the span depends on the setting of the ATWD pedestal voltage. I.e., Pedestal for the FADC = Pedestal for the ATWD. V+ in must be set to (Vpedestal - (span/2)) volts, or a few mV lower.

Place series resistors near remote sources. Capacitors near ADC.







Title	Digital Optical Module AD/DA	
Size C	Document Number <Doc>	Rev 1.1
Date: Tuesday, March 11, 2003	Sheet 4 of 15	

Nov 25, '02 GTP
Name change to eliminate naming conflict

Per criterion established July 2002 (gtp&drn) the design goal for the IceCube DOM is 200 PE = 1V into the ATWD dictated by PMT saturation behavior. Namely, the PMT NEVER delivers more than about 2V, and is linear to about 1V into a 50 ohm load (100 ohm || back-termination).

Locate these amplifiers --> close to the PMT signal input.

1*1.3*5 + 2*1.3*5 + 6.8*10 + 2*1.15*10+2*1.1*5+
3*0.4*10=134 mW
opamp comparator, 1135 8014 8014 8005

Caution: The comparators are 5V parts that cannot be operated from 3.3V. Care must be taken to protect the driven 3.3V part.

Calibration input test-point. Drive with 5V square wave to generate fixed amplitude test pulses.

Nov 22, 2001 Thorsten proposes adding R452, changing value of R108 to meet design document requirement.

SamTec SMM-102-01-S-D
Thru-Hole 2x2 2mm socket mates with SamTec TW-02-01-S-D-120-080 2x2 2mm break-away header

Dec 3, 2002 GTP Change connectors for delay line

Test pulse injection (if it doesn't work, remove transformer, and use jumper.)

If the PMT delivers 3V into a 50 ohm load, then change the divider resistors to R30=31.6 and R54=63.4 Leave the gain of the amplifier unchanged. The design goal is to have the PMT saturation voltage within the span of the ATWD.

0.47uF Y5V
Samsung CL31F474ZBNC
(0.12)

Should the ADC channel be DC coupled?

optimized for 200 MHz BW
Also try observing the performance of this stage with 499 and 249 ohm feedback divider. See if it is still as stable. It should have more bandwidth.

The shaped signal path design was from Harold Yaver of the Engineering Department.
-Modifications added to insure stable offset behavior, and to offset the output to match the input range of the ADC

Jan 19, 2003 Correct reversed polarized capacitors on analog stages. gtp

Lawrence Berkeley National Laboratory	GTP/JL/DRN/HY
Title	Digital Optical Module Analog Front End
Size C	Document Number <Doc> Rev 0
Date: Tuesday, March 11, 2003	Sheet 5 of 15

U82B

IO_Bank 12 not inc luding multi_p urpose pins

IO-*LVDSOUT05n K2 FL_TRIGGER
IO-*LVDSOUT06p L1 COM_DB6
IO-*LVDSOUT06n L2 COM_DB7
IO-*LVDSOUT07p M1 COM_DB8
IO-*LVDSOUT07n M2 COM_DB9
IO-*LVDSOUT08p R1 COM_DB10
IO-*LVDSOUT08n R2 COM_DB11
IO-*LVDSOUT09p T1 COM_DB12
IO-*LVDSOUT09n T2 COM_DB13
IO-*LVDSOUT10p U1 FL_Trigger_bar
IO-*LVDSOUT10n U2 COM_TX_SLEEP
IO-*LVDSOUT11p W1 FPGA_D0
IO-*LVDSOUT11n W2 FPGA_D1
IO-*LVDSOUT12p V1 FPGA_D2
IO-*LVDSOUT12n V2 FPGA_D3
IO-*LVDSOUT13p Y1 FPGA_D4
IO-*LVDSOUT13n Y2 FPGA_D5
IO-*LVDSOUT14p AA1 SingleLED-TRIGGER
IO-*LVDSOUT14n AA2 FPGA_D6
IO-*LVDSOUT15n AC2 FPGA_D7
IO-*LVDSOUT16p AB1 COINCIDENCE_OUT_UP
IO-*LVDSOUT16n AB2 COINCIDENCE_OUT_DOWN

IO_Bank 12

EPXA1F672I2

R393 100 C413 22pF NPO
COINC_UP_A — 1 2 — COINC_UP_ABAR
R396 100 C414 22pF NPO
COINC_UP_B — 1 2 — COINC_UP_BBAR
R86 100 C415 22pF NPO
COINC_DOWN_A — 1 2 — COINC_DOWN_ABAR
R400 100 C416 22pF NPO
COINC_DOWN_B — 1 2 — COINC_DOWN_BBAR

U82A

I/O Bank 13 not inc luding multi-p urpose pins

IO-E4_R1 E4 A_nB
IO-E3_R1 E3 FPGA_DA
IO-F3_R3 F3 FPGA_CE
IO-F4_R1 F4 HVD_IN
IO-G3_R2 G3 HVD_TxENA
IO-G4_R2 G4 HVD_RxENA
IO-H3_R2 H3 R399 100 HVD_Rx
IO-H4_R2 H4 COM_AD_OTR
IO-H5_R1 H5 COM_AD_D9
IO-J3_R3 H3 COM_AD_D8
IO-J4_R3 J4 COM_AD_D7
IO-J5_R2 J5 COM_AD_D6
IO-K3_R4 K3 COM_AD_D5
IO-K4_R3 K4 COM_AD_D4
IO-K5_R4 K5 COM_AD_D3
IO-L3_R5 L3 COM_AD_D2
IO-L4_R4 L4 COM_AD_D1
IO-L5_R4 L5 COM_AD_D0
IO-R5_R5 R5
IO-R6_R6 R6 FPGA_RW

EPXA1F672I2

U82F

IO_Bank_8

FA[0..17]
FA0 AB26 IO-*RXINCLK1p_LVDS IO-L21 L21
FA1 AB25 IO-*RXINCLK1n_LVDS IO-M22 M22
IO-M24 M24
FA2 Y26 IO-*LVDSIN01 IO-M21 M21 FL_ATTN
FA3 Y25 IO-*LVDSIN01A IO-L20 L20 FL_TCK
IO-M20 M20 FL_TDO
FA4 AA26 IO-M19 M19 FL_TDI
FA5 AA25 IO-*LVDSIN02p IO-L19 L19 FL_TMS
IO-*LVDSIN02n IO-N25 N25 FL_PRE_TRIG
IO-M23 M23 FL_Trigger
FA6 W26 IO-N23 N23 FL_Trigger_bar
FA7 W25 IO-*LVDSIN03p IO-K24 K24 nFOE
IO-*LVDSIN03n IO-L24 L24 nFWE
FA8 V26 IO-K22 K22 nFLB
FA9 V25 IO-*LVDSIN04p IO-L23 L23 nFUB
IO-*LVDSIN04n IO-L22 L22 nFCS3
FA10 U26 IO-K19 K19 nFCS2
FA11 U25 IO-*LVDSIN05p IO-K21 K21 nFCS1
IO-*LVDSIN05n IO-K20 K20 nFCS0
FA12 T26
FA13 T25 IO-*LVDSIN06p
IO-*LVDSIN06n
FA14 R26
FA15 R25 IO-*LVDSIN07p
IO-*LVDSIN07n
FA16 M26
FA17 M25 IO-*LVDSIN08p
IO-*LVDSIN08n
FD[0..15]
FD0 L26 IO-*LVDSIN09p
FD1 L25 IO-*LVDSIN09n
FD2 K26 IO-*LVDSIN10p
FD3 K25 IO-*LVDSIN10n
FD4 J26 IO-*LVDSIN11p
FD5 J25 IO-*LVDSIN11n
FD6 H26 IO-*LVDSIN12p
FD7 H25 IO-*LVDSIN12n
FD8 G26 IO-*LVDSIN13p
FD9 G25 IO-*LVDSIN13n
FD10 F26 IO-*LVDSIN14p
FD11 F25 IO-*LVDSIN14n
FD12 E26 IO-*LVDSIN15p
FD13 E25 IO-*LVDSIN15n
FD14 D26 IO-*LVDSIN16p
FD15 D25 IO-*LVDSIN16n

3.3V
1K 1% R209 R210 R211 R212 R277 R278 R279

EPXA1F672I2

EB_nCS0 R394 4.7K
EB_nCS1 R395 4.7K
EB_nCS2 R397 4.7K
EB_nCS3 R398 4.7K
3.3V

U82H

Flash Chip Select r outed through PLD

IO_Bank_6

Exten sion Bus Inter face

EBA[0..24]
EBA0 F20 EBI_A0
EBA1 C21 EBI_A1
EBA2 E20 EBI_A2
EBA3 H18 EBI_A3
EBA4 G19 EBI_A4
EBA5 J18 EBI_A5
EBA6 J17 EBI_A6
EBA7 G18 EBI_A7
EBA8 D20 EBI_A8
EBA9 F19 EBI_A9
EBA10 H17 EBI_A10
EBA11 E19 EBI_A11
EBA12 C20 EBI_A12
EBA13 D19 EBI_A13
EBA14 F18 EBI_A14
EBA15 C19 EBI_A15
EBA16 G17 EBI_A16
EBA17 K15 EBI_A17
EBA18 D18 EBI_A18
EBA19 E18 EBI_A19
EBA20 H16 EBI_A20
EBA21 F17 EBI_A21
EBA22 C18 EBI_A22
EBA23 J16 EBI_A23
EBA24 E17 EBI_A24 See Errata->

EBI_CS0 K17 EB_nCS0
EBI_CS1 H20 EB_nCS1
EBI_CS2 J19 EB_nCS2
EBI_CS3 G20 EB_nCS3
EBI_OE_N C22 EB_nOE
EBI_WE_N E21 EB_nWE
EBI_BE0 D22
EBI_BE1 K18
EBI_DQ0 C17 EBD0
EBI_DQ1 G16 EBD1
EBI_DQ2 D17 EBD2
EBI_DQ3 E16 EBD3
EBI_DQ4 J15 EBD4
EBI_DQ5 E15 EBD5
EBI_DQ6 G15 EBD6
EBI_DQ7 H15 EBD7
EBI_DQ8 E15 EBD8
EBI_DQ9 J14 EBD9
EBI_DQ10 E14 EBD10
EBI_DQ11 K14 EBD11
EBI_DQ12 G14 EBD12
EBI_DQ13 F14 EBD13
EBI_DQ14 H14 EBD14
EBI_DQ15 EBD15
EBI_CLK D21 EB_CLK
INT_EXT_PIN_N H19 INT_EXT_PIN_N
EBI_ACK K16

EB_nCS[0..3]
EBD[0..15]

EPXA1F672I2

U82K

IO_Bank_2

SD RAM Bus

A[0..14]
A0 K9 SD_A0
A1 C5 SD_A1
A2 E6 SD_A2
A3 G6 SD_A3
A4 K8 SD_A4
A5 A4 SD_A5
A6 B4 SD_A6
A7 F5 SD_A7
A8 D5 SD_A8
A9 G5 SD_A9
A10 K11 SD_A10
A11 E5 SD_A11
A12 H8 SD_A12
A13 J8 SD_A13
A14 F6 SD_A14

SD_CLK B5 SD_CLK
SD_CLK_N G7 SD_nCLK
SD_CLKE F7 SD_CLKE
SD_CS_N1 D6 SD_CS_N1
SD_CS_N0 E7 SD_CS_N0
SD_RAS_N J9 nRAS
SD_CAS_N F8 nCAS
SD_WE_N A5 nWE
SD_DQS0 F12 SD_nCLK
SD_DQS1 H11
SD_DQS2 J10
SD_DQS3 K10
SD_DQM0 H12 SD_DQM0
SD_DQM1 G11 SD_DQM1
SD_DQM2 F9 SD_DQM2
SD_DQM3 C6 SD_DQM3

SD_CS_N[0..1]
See HW Ref Manual
NC
SD_DQM[0..3]

J13 D0
SD_DQ0 H13 D1
SD_DQ1 E11 D2
SD_DQ2 G13 D3
SD_DQ3 E13 D4
SD_DQ4 D13 D5
SD_DQ5 C13 D6
SD_DQ6 B12 D7
SD_DQ7 E12 D8
SD_DQ8 G12 D9
SD_DQ9 J12 D10
SD_DQ10 A12 D11
SD_DQ11 C12 D12
SD_DQ12 A11 D13
SD_DQ13 K13 D14
SD_DQ14 A10 D15
SD_DQ15 A9 D16
SD_DQ16 H10 D17
SD_DQ17 B8 D18
SD_DQ18 C9 D19
SD_DQ19 E9 D20
SD_DQ20 K12 D21
SD_DQ21 D9 D22
SD_DQ22 G9 D23
SD_DQ23 D8 D24
SD_DQ24 H9 D25
SD_DQ25 A7 D26
SD_DQ26 B7 D27
SD_DQ27 E8 D28
SD_DQ28 G8 D29
SD_DQ29 C7 D30
SD_DQ30 D7 D31
SD_DQ31

D[0..31]

nc-SD_DQ_ECC0 G10
nc-SD_DQ_ECC1 J11
nc-SD_DQ_ECC2 C10
nc-SD_DQ_ECC3 C11
nc-SD_DQ_ECC4 E10
nc-SD_DQ_ECC5 D11
nc-SD_DQ_ECC6 F11
nc-SD_DQS_ECC F10
nc-SD_DQM_ECC G11
DDR_VS0 D12
DDR_VS1 E11
DDR_VS2 C8

EPXA1F672I2

If the FE_TES T_PULSE --> line in jects objectionable noise into the front, t hen perhaps that could b e mitigated by making it drive differen tially.

DO NOT CH ANGE PIN ASSIGNMENTS O F AC8, AD7, AD8, AE7. These pin assignments chosen to optimize sp eed. gtp 9/11/02

U82C

IO_Bank 11

ATWDTrigger_0 AB8 IO-AB8_C1
nSPE AC8 IO-AC8_C2
ATWDTrigger_1 AD7 IO-AD7_C2
MultiSPE AE7 IO-AE7_C3
MultiSPE-nL AD8 IO-AD8_C3
COINC_DOWN_ALATCH AC9 IO-AC9_C4
COINC_DOWN_ABAR AE9 IO-AE9_C4
COINC_DOWN_A AA10 IO-AA10_C5
COINC_DOWN_BLATCH AD9 IO-AD9_C5
COINC_DOWN_BBAR AB9 IO-AB9_C6
COINC_DOWN_B AC10 IO-AC10_C6
COINC_UP_ALATCH AF9 IO-AF9_C7
COINC_UP_A AB10 IO-AB10_C7
COINC_UP_ABAR AE10 IO-AE10_C8
COINC_UP_BLATCH AA11 IO-AA11_C8
COINC_UP_BBAR AD10 IO-AF10_C9
COINC_UP_B AD10 IO-AD10_C9
FLASH_AD_D0 AB11 IO-AB11_C10
FLASH_AD_D1 AC11 IO-AC11_C10
FLASH_AD_D2 AD11 IO-AD11_C11
FLASH_AD_D3 AF11 IO-AF11_C11
FLASH_AD_D4 AA12 IO-AA12_C12
FLASH_AD_D5 AB12 IO-AB12_C12
FLASH_AD_D6 AE11 IO-AE11_C13
FLASH_AD_D7 AC12 IO-AC12_C13
FLASH_AD_D8 AD12 IO-AD12_C14
FLASH_AD_D9 AC13 IO-AC13_C14
FLASH_NC3 AB14 IO-AB14_C15
AA13 IO-AA13_C15
FLASH_AD_STBY AB13 IO-AB13_C16

EPXA1F672I2

ATWD1VDD-SUP
ATWD0VDD-SUP
R369 10K 1%
R368 10K 1%

U62E

IO_Bank 9 not inc luding multi_p urpose pins

IO-AD22 AD22 R2BUS0
IO-AC22 AC22
IO-AC25 AC25 FE_TEST_PULSE
IO-AC26 AC26
IO-AB19 AB19 OneSPE-nL
IO-AB20 AB20 R2BUS2
IO-AB21 AB21 R2BUS1
IO-AB22 AB22
IO-AB23 AB23
IO-AB24 AB24
IO-AA19 AA19
IO-AA20 AA20 R2BUS3
IO-AA21 AA21 R2BUS4
IO-AA22 AA22
IO-AA23 AA23
IO-AA24 AA24
IO-Y19 Y19 R2BUS5
IO-Y20 Y20 R2BUS6
IO-Y21 Y21
IO-Y22 Y22
IO-Y23 Y23
IO-Y24 Y24 R2BUS[0..6]
IO-W20 W20
IO-W21 W21
IO-W22 W22 FE_PULSER0p
IO-W23 W23 FE_PULSER0n
IO-W24 W24
IO-V19 V19 PLD_FPGA_nOE
IO-V20 V20 PLD_FPGA_nWE
IO-V21 V21 PLD_FPGA_BUSY
IO-V22 V22 FE_PULSER1p PLD_FPGA[0..7]
IO-V23 V23 FE_PULSER1n
IO-V24 V24 PLD_FPGA7
IO-U20 U20 PLD_FPGA6
IO-U21 U21 FE_PULSER2p PLD_FPGA5
IO-U22 U22 FE_PULSER2n PLD_FPGA4
IO-U23 U23 PLD_FPGA3
IO-T20 T20 PLD_FPGA2
IO-T21 T21 FE_PULSER3p PLD_FPGA1
IO-T22 T22 FE_PULSER3n PLD_FPGA0
IO-T24 T24
IO-R20 R20

EPXA1F672I2

U82L

A2 GND
A8 GND
A10 GND
A14 GND
A17 GND
A18 GND
A25 GND
B1 GND
B2 GND
B6 GND
B13 GND
B21 GND
B25 GND
B26 GND
C3 GND
C24 GND
D6 GND
D23 GND
L11 GND
L16 GND
M12 GND
M15 GND
M17 GND
N1 GND
N4 GND
N11 GND
N13 GND
N14 GND
N16 GND
N18 GND
N26 GND
P1 GND
P2 GND
P3 GND
P13 GND
P14 GND
P16 GND
P23 GND
P26 GND
R12 GND
R15 GND
R17 GND
T11 GND
T13 GND
T14 GND
T16 GND
T18 GND
U10 GND
U12 GND
U17 GND
V9 GND
V18 GND
W8 GND
W19 GND
AC4 GND
AC23 GND
AD3 GND
AD24 GND
AE1 GND
AE2 GND
AE6 GND
AE13 GND
AE21 GND
AE25 GND
AF6 GND
AF2 GND
AF8 GND
AF14 GND
AF19 GND
AF25 GND

R8 GND_CKLK4 Vcc_CKLK4
T9 GND_CKLK2 Vcc_CKLK2
F23 GND_CKLK6 Vcc_CKLK6
F22 GND_CKLK5 Vcc_CKLK5
V8 GND_CKOUT2 VccCKOUT2

A1 Vccint
A24 Vccint
B3 Vccint
B8 Vccint
B10 Vccint
B17 Vccint
B19 Vccint
B24 Vccint
C1 Vccint
C2 Vccint
C4 Vccint
C23 Vccint
C25 Vccint
C26 Vccint
D3 Vccint
D24 Vccint
L13 Vccint
L15 Vccint
M13 Vccint
M16 Vccint
N2 Vccint
N10 Vccint
N12 Vccint
P15 Vccint
P18 Vccint
P24 Vccint
P25 Vccint
R10 Vccint
R11 Vccint
R14 Vccint
T12 Vccint
T17 Vccint
U9 Vccint
U14 Vccint
U16 Vccint
AC3 Vccint
AC24 Vccint
AD1 Vccint
AD2 Vccint
AD4 Vccint
AD22 Vccint
AD25 Vccint
AE3 Vccint
AE8 Vccint
AE18 Vccint
AE23 Vccint
AE24 Vccint
AF3 Vccint
AF24 Vccint

1.8V

C91 OSCON 6SC47M From Sany o Video C92 OSCON 6SC47M
C93 C94 470pF NPO 470pF NPO
C95 C101 100nF 100nF

gtp 10N L 9/3/2002

I/O bank used by SDRAM memory.

I/O bank used by Flash memory.

Vccio_2 B14 Vccio_2 P11 Vccio_2 U15
Vccio_3 P17 Vccio_3 R18 Vccio_3 U13
Vccio_6 A6 Vccio_6 L12 Vccio_6 L14
Vccio_7 A13 Vccio_7 M14 Vccio_7 N17
Vccio_8 A21 Vccio_8 L17 Vccio_8 N15 Vccio_8 N24
Vccio_9 R16 Vccio_9 U18
Vccio_10 T15 Vccio_10 V17 Vccio_10 AE14 Vccio_10 AF21
Vccio_11 R13 Vccio_11 U11 Vccio_11 V10 Vccio_11 AF13
Vccio_12 T10 Vccio_12 AF6 Vccio_12 M11 Vccio_12 N3 Vccio_12 C12
Vccio_13 R9 Vccio_13 T8 Vccio_13 F23 Vccio_13 E22 Vccio_13 AD23 Vccio_13 U8

3.3V
C417 C379 C380 470pF NPO 100nF OSCON 6SC47M
C345 C346 C315 100nF OSCON 6SC47M 470pF NPO
C347 C348 C349 470pF NPO 100nF OSCON 6SC47M
C370 C299 C300 470pF NPO 100nF OSCON 6SC47M
C204 C207 C301 470pF NPO 100nF OSCON 6SC47M
C213 C214 C305 470pF NPO 100nF OSCON 6SC47M
C223 C310 C224 C226 C297 100nF OSCON 6SC47M 470pF NPO 470pF NPO
C217 470pF NPO
C237 C263 C296 470pF NPO 100nF OSCON 6SC47M
C424 C425 C426 470pF NPO 100nF OSCON 6SC47M

R263 Open Ckt
R258 Open Ckt I/O bank use d by SDRAM. Support optional I/O voltages.
R259 Jumper

2.5V
Jumper
JU5
JU6
3.3V
Open Ckt

EPXA1F672I2

Connect all the NO_CONNECT pins to an obstacle o n a plane that WILL NOT map to a gerber layer. This insures tha t all the pins are connected t o pads, so are access able.

U82M

D2 NC
E2 NC
F2 NC
F4 NC
G2 NC
H2 NC
H3 NC
J2 NC
J3 NC
K2 NC
K3 NC
L2 NC
L3 NC
L4 NC
L13 NC
L17 NC
M2 NC
M3 NC
M4 NC
M11 NC
M14 NC
N2 NC
N3 NC
N4 NC
N12 NC
N13 NC
P2 NC
P3 NC
P4 NC
P12 NC
P13 NC
R2 NC
R3 NC
R4 NC
R13 NC
T2 NC
T3 NC
T4 NC
T12 NC
T13 NC
NC

NC
J3
J4
J5
J6
J7
J9
J10
J11
J12
J13
J14
J15
K4
K5
K6
K7
K9
K10
K11
K12
K13
K14
K15
L5
L6
L7
L8
L9
L10
L11
L12
M5
M6
M7
M8
M9
M10
M12
N5
N6
N7
N8
N9
N10
N11
P5
P6
P7
P8
P9
P10
P11
R5
R6
R7
R8
R9
R10
R11
R12
T5
T6
T7
T8
T9
T10
T11

EPXA1F672I2

U82D

IO_Bank 10 not inc luding multi_p urpose pins

IO-AA14 AA14 TriggerComplete_0
IO-W14 W14 OutputEnable_0
IO-W15 W15 CounterClock_0
IO-Y15 Y15
IO-AC14 AC14 ATWD0_D0 ShiftClock_0
IO-V15 V15
IO-AD15 AD15 ATWD0_D1 RampSet_0
IO-AC15 AC15
IO-AB15 AB15 ATWD0_D2 ChannelSelectMSB_0
IO-AA15 AA15
IO-AF16 AF16 ATWD0_D3 ChannelSelectLSB_0
IO-AE16 AE16
IO-AD16 AD16 ATWD0_D4 ReadWrite_0
IO-AB16 AB16
IO-AC16 AC16 ATWD0_D5 AnalogReset_0
IO-AA16 AA16
IO-V16 V16 ATWD0_D6 DigitalReset_0
IO-W16 W16
IO-Y16 Y16 ATWD0_D7 DigitalSet_0
IO-AF17 AF17
IO-AE17 AE17 ATWD0_D8
IO-AD17 AD17
IO-AC17 AC17 ATWD0_D9 TriggerComplete_1
IO-W17 W17 OutputEnable_1
IO-AB17 AB17 CounterClock_1
IO-AA17 AA17 ATWD1_D0 ShiftClock_1
IO-Y17 Y17
IO-AF18 AF18 ATWD1_D1 RampSet_1
IO-AE18 AE18
IO-AB18 AB18 ATWD1_D2 ChannelSelectMSB_1
IO-Y18 Y18
IO-AD18 AD18 ATWD1_D3 ChannelSelectLSB_1
IO-AD19 AD19
IO-AC20 AC20 ATWD1_D4 ReadWrite_1
IO-AD20 AD20
IO-AC19 AC19 ATWD1_D5 AnalogReset_1
IO-AC18 AC18
IO-AE22 AE22 ATWD1_D6 DigitalReset_1
IO-W18 W18
IO-AA18 AA18 ATWD1_D7 DigitalSet_1
IO-AA19 AC23
IO-AE23 AD21 ATWD1_D8
IO-AD21 AE20 ATWD1_D9
IO-AE20 AF20
IO-AF20 AC21
IO-AC21

10K 1% R207 10K 1% R204 10K 1% R201 10K 1% R198 10K 1% R195 10K 1% R192 10K 1% R189
10K 1% R206 10K 1% R203 10K 1% R200 10K 1% R197 10K 1% R194 10K 1% R191
10K 1% R205 10K 1% R202 10K 1% R199 10K 1% R196 10K 1% R193 10K 1% R190 10K 1% R187
3.3V

ATWD0_D[0..9]
ATWD1_D[0..9]

EPXA1F672I2

FE_PULSER0p R183 51 R192 24.9 R115 12.4
FE_PULSER1p R216 51 R275 24.9 R117 12.4
FE_PULSER2p R215 51 R248 24.9 R181 12.4
FE_PULSER3p R182 51 R255 24.9 R184 24.9
FE_PULSER3n R188 51 R254 24.9 R249 24.9 R185 1
FE_PULSER2n R162 51 R252 24.9 R55 12.4 R163 12.4
FE_PULSER1n R164 51 R251 24.9 R165 12.4
FE_PULSER0n R186 51 R250 24.9

T8 Mini-Circuits TCM1-1
VRef
Inject-
TP8
TP*

Multiplexed Calib ration Inputs:
Toyocom Osc for capture rate calibra tion, and absolute phase reference
CLK Osc 40 MHz system clock
Flash current waveform fo r LED on DOM Main Board
Flash current waveform for LED daughter board
Local Coincidence Signa l from upper neighbor
Local Coincidence Signa l from lower neighbor
Communications Signal for re lative phase of time ticks
Communications Signal for re lative phase of time ticks

For best integrity of cal ibration, mount the two MAX4141 chips such that th e 20 ohm resistor outputs abut, and pin 11 to the 20 ohm resistor is the same length, and leads to inputs are kept short since they are high freque ncy carriers.

If noise is being coupled t hrough, then p ut a resistor or bead here.

Power B udget
50 + 50 + 1 + 5.1 + 5.1 + 4.25 + 4.25 + 2xATWD ea

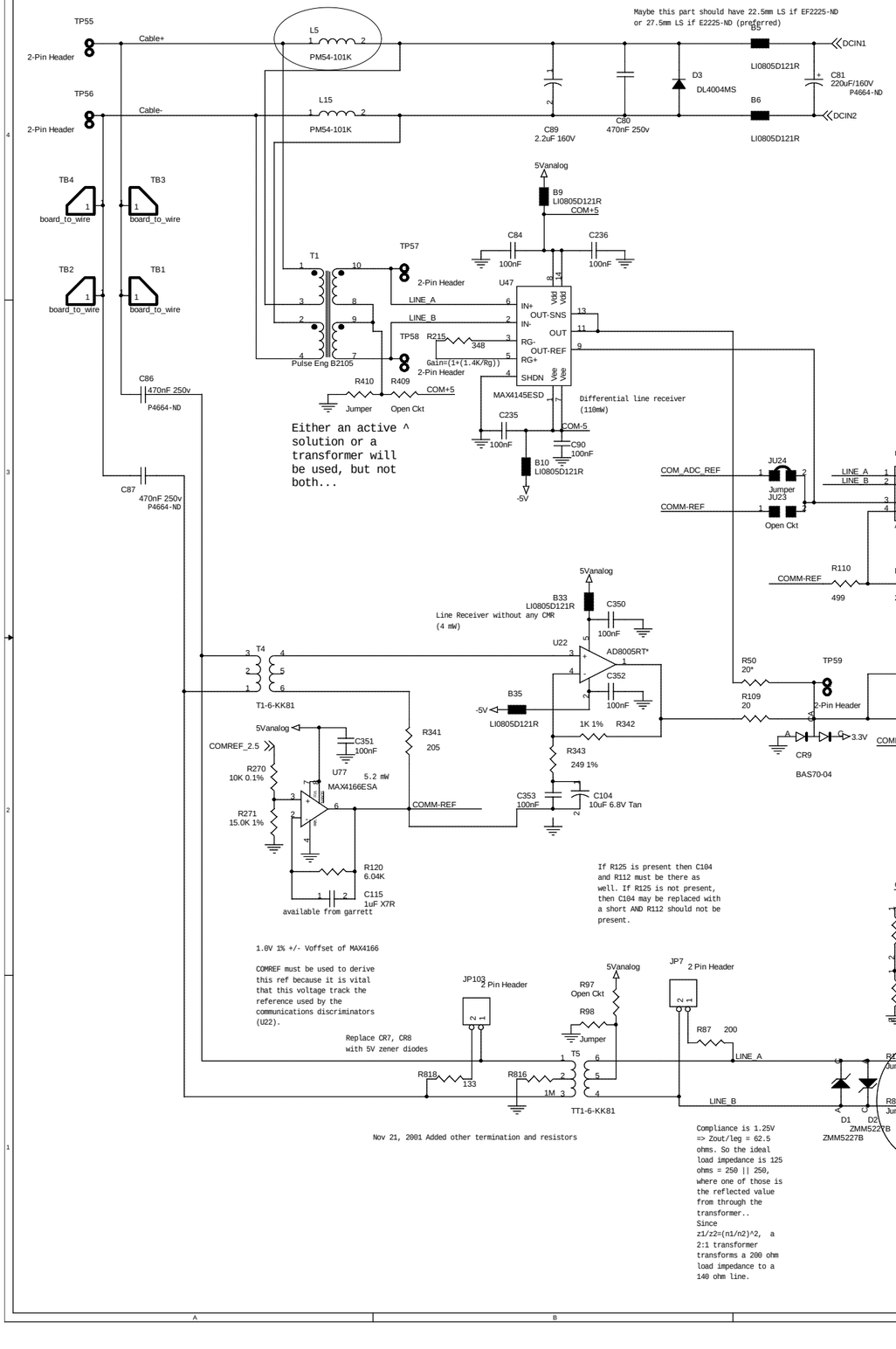
Could be a lower powe r part with greater delay, like max998, if it is necessary to save 6ma.

1.65V

SEMICONWELL 29 64-2966 Scott Blvd. Santa Cl ara, CA 95054 Tel:(408) 986-0826 Fax:(408)-85 0-1911, or equiva lent.

Use a low voltage driving stan dard. Wired to a low vo ltage I/O bank of t he FPGA

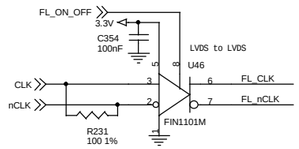
Title	Digital Optical Module ATWD	
Size D	Document Number <Doc>	Rev <RevCode>
Date: Tuesday, March 11, 2003	Sheet 7 of 15	

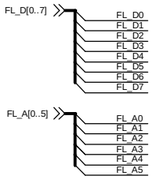


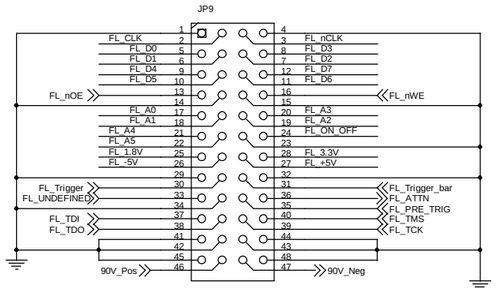
Title: Digital Optical Module Communication

Size	Document Number	Rev
C	<Doc>	<RevCode>

Date: Tuesday, March 11, 2003 Sheet 8 of 15







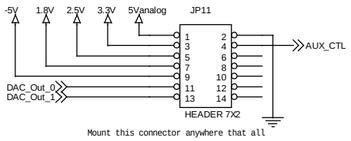
12 x 4 SamTec ESQT-112-02-L-Q-078

Looking down on the component side of the DOM main PCB the pin pattern will look like the image above

1	GND
2	CLK
3	CLK\
4	GND
5	FL_D0
6	FL_D1
7	FL_D2
8	FL_D3
9	FL_D4
10	FL_D5
11	FL_D6
12	FL_D7
13	RD\
14	GND
15	GND
16	WR\
17	FL_A0
18	FL_A1
19	FL_A2
20	FL_A3
21	FL_A4
22	FL_A5
23	GND
24	ON/OFF
25	1.8V
26	+5V
27	-5V
28	3.3V
29	GND
30	TRIG
31	TRIG\
32	GND
33	Undefined
34	GND
35	PRE_TRIG
36	FL_ATTN
37	TDI
38	TDO
39	TCK
40	TMS
41	GND
42	GND
43	GND
44	GND
45	GND
46	90V_Pos
47	90V_Neg
48	GND
45	GND

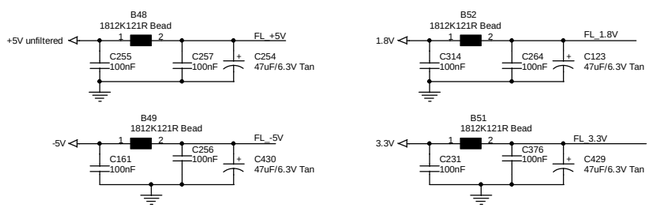
In the 4x10 arrangement, this looks like the following:

GND	FL_D0	FL_D4	RD\	FL_A0	FL_A4	1.8V	GND	Undef	TDI	GND	GND
CLK	F L_D1	FL_D5	GND	FL_A1	FL_A5	+5V	TRIG	GND	TDO	GND	90V Pos
CLK\	F L_D2	FL_D6	GND	FL_A2	GND	-5V	TRIG\	PRE_TRIG	TCK	GND	90V_Neg
GND	FL_D3	FL_D7	WR\	FL_A3	ON/OFF	3.3V	GND	ATTN	TMS	GND	GND

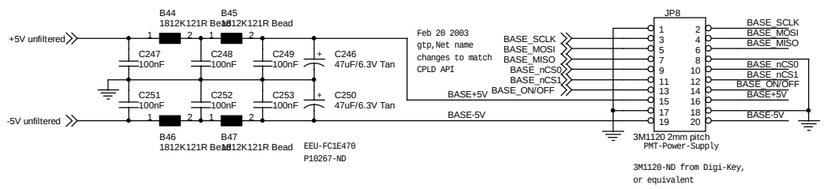


Mount this connector anywhere that all power supply voltages are available.

Can be used to power and control alternate PMT power supply

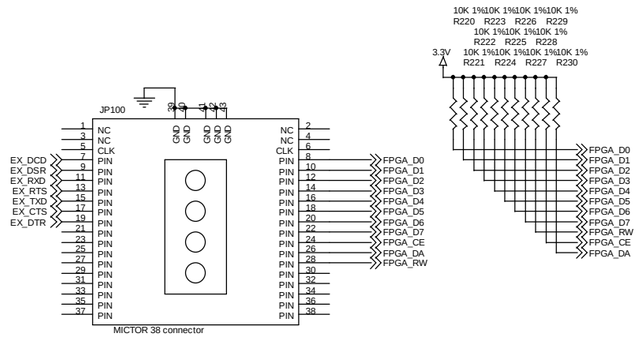


2/9/2003 gtp Voltage nets, NOT off page connectors.

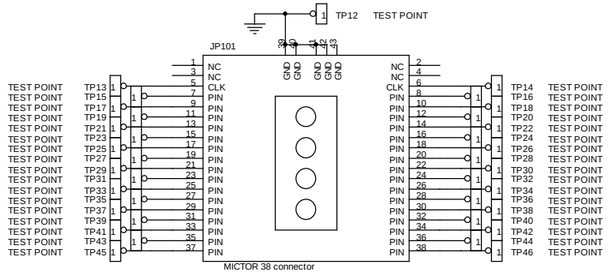


1	GND
2	SCK - Serial clock
3	SCK
4	MOSI -Serial data in
5	MOSI
6	MISO - Serial data out
7	MISO
8	GND
9	CS0 (DAC) - Chip select for DAC
10	CS0
11	CS1 (ADC) - Chip select for ADC
12	CS1
13	ON/OFF - Power supply enable/disable
14	ON/OFF
15	+5V - Main power
16	+5V
17	GND
18	GND
19	-5V - Main power
20	-5V

to match the interface document, Jan 02, '03



Compatible with model P6434 probe for Tektronix logic analyzer.



This connector is meant to be used during pre-production debugging. The footpring should be mounted on a part of the board that is later broken off and discarded. The test-points will be used to tack down one of wires that bring signals out of the main board.

Compatible with model P6434 probe for Tektronix logic analyzer.

Title	Off-Board Subsystems		
Size C	Document Number <Doc>		Rev <RevCode>
Date: Tuesday, March 11, 2003		Sheet 9 of 15	

Design for 1V output swing of driver=>0.5 V at port =>0.3535V at sum por t.
0.3535V from neighbor at sum port => 0.175 V at port B => 0.87V threshol d.
Tune with resistor between bases of Q21, Q22.

Drive this node with Tri-State output of F PGA.
A pull-up will deliver a positive unit pu lse.
A pull-down will deliver a negative unit pu lse.

Balanced output to minimise noise on the board during an e vent.

Note to FPGA designe r:
'COINCIDENCE_OUT_N xx lines must 'float' wh en not signaling (i e high-Z state o f tri-state output) . Both positive an d negative pulses a re permitted by pulling up or down on the inpu ts to the driver op-amp s.

I good four quadrent low power 1.65V reverence could be used in place of the MAX4166 and associ ated circuitry. A potential problem for this circu it is the stability of the MAX4161 when either or bo th of the opamps are driven. Varify with first proto type.

Nov 21, 2001 Bob add ed 1M resistors t o transformers .

Power = 4*1.3*5 + 2*0.4*5 + 1*1.3*5 = 36 mW

T3-1T-K81
A balanced waveform, like AMI, is desirable for transmission over t his pathway.

T3-1T-K81
It may be possible to repla ce the PSC-2-2 with a simp le transformer, but this requir es taking into account impedan ce matching side-effects. In a ny case, T2, T3 will have to be chosen to match the splitter to the twisted pair cable .

CAUTION
Gnd of PSC-2-2 operate s at pedestal potentia l

Thresholds should b e +/- 0.08V or s o above and belo w COINC_REF.

Make sure that when the op-am ps are driven, there is n o significant bounce on t he 'ground' pins of the pow er splitters.

Title	Digital Optical Module Local Coincidence
Size B	Document Number <Doc>
Rev	0
Date:	Tuesday, March 11, 2003
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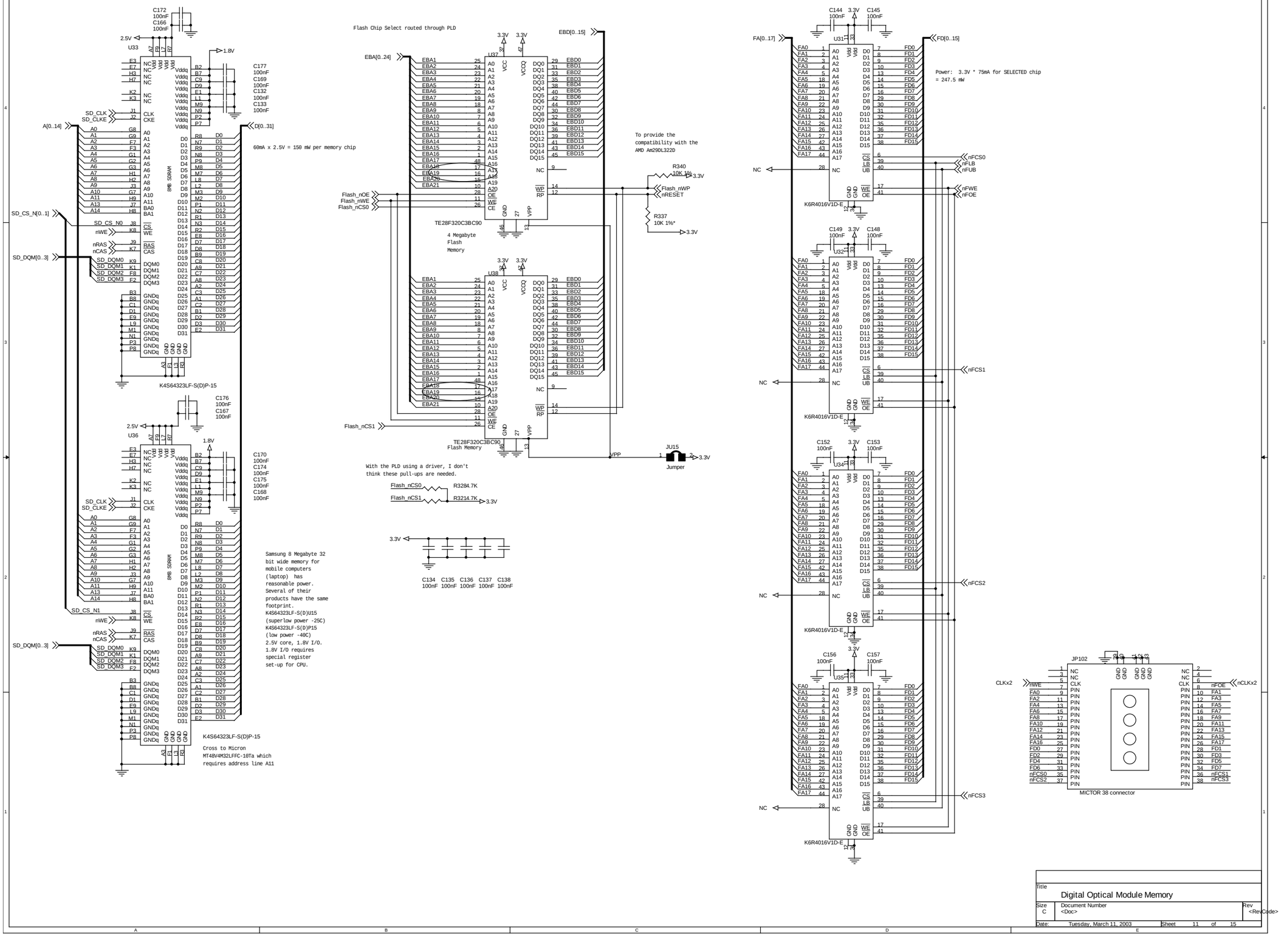

Title	Digital Optical Module Memory
Size: C	Document Number: <Doc>
Rev	<RevCode>
Date:	Tuesday, March 11, 2003
Sheet	11 of 15

Require MUX_ENA low at power up.
Require HV power supply control
at power up, and through
reloading the FPGA.
BOOT_FLASH line control

Desire:
ADC and DAC control not
depending on FPGA load (avoid
glitches)
remember source of power failure
Flash Memory CSR remapping

If the communications ADC and DAC do not load the near by translator too heavily, and if the line to the CPLD is short, then U78 may be taken out of the design, and the clock line routed to the GCLK0 line of the CPLD.

An address space of 16 registers

Monitor ADC (i2c) AD/DA Page

Clk line for SPI/Microwire & I2c

ATWD1 DAC

ATWD0 DAC

Output used to unconfigure FPGA

Bank 2 - Bank 1 - Bank 2 - Bank 2 - Bank 2 - Bank 2 - Bank 1 - Bank 1 - Bank 1 - Bank 1 - Bank 1 - Bank 1

XC2C256_TQ144

EPXA1F672I2

CPU-CLK is a clock that HAS to be there at power up. FPGA-CLK must be delivered to the FPGA after the FPGA is configured (a documented work-around) or a late version of Quartus must be used to compile.

Might want to add some of these nets to the NC net.

nCE = pull-down
nCEO = open ckt
TRST = pull-up
TDI = pull-up
TDO = pull-up
TMS = pull-up
TCK = pull-up
nSTATUS = pull-up
CONFIG_DONE = pull-up
nCONFIG = pull-up

Service Connector for the convenience of software programmers. Utilizes multifunction pins.

Feb 10, 2003 GTP -TEST_MODE Jumper.
Feb 3, 2003 gtp Approved Feb 5

bas16-sot0 comp property

Feb 20, 2003 gtp Net Name Changes for CPLD.

Feb 6, 2003 gtp

Feb 3, 2003 gtp Approved Feb 5

This forces the power supply to crash, initiating power on reset nPOR after a time delay.

Feb 3, 2003 gtp Approved Feb 5

B3FS-1002P (Omron)

WideAreaFlasherBoard

Verticle Entry Shrowded header

Per Lantronix Server documentation

Wired as DTE
Use 1:1 cable to MODEM

Feb 3, 2003 gtp
Silk screen shows wrong direction.

If it is found that the configuration is correct, JU11, and JU12 can be installed during manufacture.

For bypassing the EPC2, jumper center to bridging position, pin 1 to pin 2. To put EPC2 into circuit, jumper pin1 to pin3, and pin2 to pin 4.

DO not mount PRC_JTAG connector

Title	Digital Optical Module CPU		
Size C	Document Number <Doc>		Rev <RevCode>
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Charge pump voltage doub ler driven by a buffer driven by a DAC output.

B32

5Vanalog

LI0805D121R

C291

100nF

5.1 mW

SingleLED-BRIGHTNESS-CTL

Driven by a 10 bit DAC

U70

MAX4166ESA

R237 10

R239

100

U69

0.6 mW

C239

2.2uF 6.3V Tan

FC V+

CAP+ OSC

GND LV

CAP- OUT

MAX660ESA

C242

10uF 6.8V Tan

TP11

2-Pin Header

C240

2.2uF 16V Tan

R235

100K 1%

C241

22pF NPO

R236

Jumper

The resistors shoul d be placed radially at one e nd of the charge storage cap acitor. The inductances should be kept as small a s possible.

Resistor values sma ller than 1 ohm are availa ble in the 1% set. Resis tors should be chosen to pr oduce an acceptable signal t o the ATWD.

R238

C244

100

100nF

C243

100nF

R243

1K 1%

Q6

MMBTH81

R244

4.7K

Q18

2N7002

DS1

UV LED

Q17

2N7002

R240 3.3

R241 3.3

R242 3.3

R234

51

PMT_LED_PULSER

TP10

2-Pin Header

R247

1K 1%

U42

R246

4.7K

C245

47pF NPO

SingleLED-TRIGGER

Z=50 ohm transmi ssion line

C232

1nF NPO

R245

1K 1%

NC7SZ14M5

SN74AHC1G1 4DBVR

Trigger on RISING ed ge. Pulse w idth >20 n s.

Title: Digital Optical Module Single LED		
Size: A	Document Number: <Doc>	Rev: 0
Date: Tuesday, March 11, 2003	Sheet 13 of 15	

Over-Voltage protection for the power supply. I suppose, this could as easily be balanced, using just the N and P FETs. If it is deemed that the power supply input voltage range (and tolerence) is great enough, the protection circuit can be deleted from the design.

At bob's suggestion, put the power pins in the yet bigger flasher board interface...

90V_Pos

90V_Neg

approved Feb 3, 2003 gtp

Current contenters are:

Polytron LWA19-90-5 (a ten watt part)
Power One 70 IMX4-0505-9 (a 4 watt part)

The winner may not be from this list.

DCIN1

DCIN2

Digi-Key Panasonic PK1064-ND ELF-15N002A

B22 1812K121R Bead

B26 1812K121R Bead

L10

ELF-15N002A

C407 100nF

!! This part is 8 ohms per leg!!

BZX84C6V8DICT-ND

C85 2.2uF 160V

C178 470nF 250v

L13 2.2mH API 2474 series

L11 2.2mH API 2474 series

C88 2.2uF 160V

NOVAcap 1812Z474M251NX 250V Z5U Ceramic Capacitor

CR4 CMHZ5263B

CR5 CMHZ5263B

<-- 112V -->

R315 10M

R316 10K 1%

Q19 2N7002

CR2 CMHZ5235B

Q13 IRF644NS

BZX84C6V8DICT-ND

JP15 HEADER 4X2*

For development: A daughter card plugged into JP15 can be used to design an appropriate filter network.

B23 1812K121R Bead

B27 1812K121R Bead

C375 470nF 250v

C179 470nF 250v

PS1 70 IMX4-0505-9 Power-One

Vin+ Vin+ 40-120V Vin- Vin-

+5V COM -5V

+5V unfiltered

R285 0.100

-5V_supply

R151 0.100

-5V unfiltered

B24 1812K121R Bead

B28 1812K121R Bead

B25 1812K121R Bead

B29 1812K121R Bead

5Vanalog

-5V

C180 100nF C181 100nF C182 100nF C234 47uF/6.3V Tan

C183 100nF C184 100nF C185 100nF C238 47uF/6.3V Tan

EEU-FC1E470 P10267-ND

EEU-FC1E470 P10267-ND

C187 OSCON_6SC6R8M +3.3V_IN

C195 OSCON_6SC6R8M +1.8V_IN

C221 OSCON_6SC6R8M +5V unfiltered

C398 OSCON_6SC6R8M +2.5V_IN

+5V unfiltered

R116 0.100 C190 100nF

R283 0.100 C198 100nF

R282 0.100 C403 100nF

R389 100K 1%

R160 100K 1%

R158 Open Ckt

R413 Jumper R153 Open Ckt R154 100K 1% R155 Open Ckt

approved Feb 3, 2003 gtp

OUT1

nPOR

nURESET

Alternet power down-reset option.

U56

INP1 INP2 INP3 Vdd DBI LBI LBO RSO OUTOK ON2 MR PGM3 REF GND GND PG3 PG2 PG1

MAX1702BEGX

The MAX1702 contains voltage monitoring circuitry, and staged start circuitry that might make the voltage monitor chip, the LTC1727, unnecessary.

L9 PM54-100M 10uH

L2 4.7uH

C186 OSCON_6SC10M

B31 1812K121R Bead

C364 47uF/6.3V Tan

LX1 OUT1 COMP1

C366 100nF

R157 33K

C191 33pF NPO

C193 1nF NPO

C362 100nF C189 100nF C196 100nF

3.3V

L3 4.7uH

C194 OSCON_6SC10M

L6 PM54-100M 10uH

B34 1812K121R Bead

C365 47uF/6.3V Tan

C402 100nF C188 100nF

LX2 FB2

R159 23.7K 1%

R388 15.0K 1%

C367 100nF

C363 100nF C197 100nF

1.8V

R152 18K

C404 33pF NPO

C201 680pF NPO

COMP2

L4 4.7uH

C396 OSCON_6SC10M

L1 PM54-100M 10uH

B38 1812K121R Bead

C397 47uF/6.3V Tan

C200 100nF C192 100nF

LX3 OUT3

C399 100nF

C400 100nF C401 100nF

2.5V

R156 22K

C199 33pF NPO

C406 1nF NPO

COMP3

C405 100nF

OSCON_6SC6R8M C321 C427 C339 C337 C335

5Vanalog

C322 C324 C326 C328 C330

-5V

C332 C334 C336 C338 C340

C333 OSCON_6SC6R8M C331 OSCON_6SC6R8M C329 OSCON_6SC6R8M C327 OSCON_6SC6R8M C325 OSCON_6SC6R8M

Distribute widely around the PC board to improve noise suppression. If noise performance is good enough, some of these parts may be deleted from the final design. The design might benefit by additional bypassing on 3.3V.

U39 AD626AR

-5V unfiltered -5V_supply 5Vanalog

C118 100nF

Imon-5V

Assuming a 500 mW load on -5V, a gain of 100 yields a 1V signal to the ADC input.

U49 AD626AR

+5V unfiltered +5V 5Vanalog

C116 100nF

Imon+5V

Assuming a 200 mW load on +5V, a gain of 100 yields a 400mV signal to the ADC input.

U50 AD626AR

+5V unfiltered +3.3V_IN 5Vanalog

C117 100nF

Imon+3.3V

Assuming a 500 mW load on +3.3V, a gain of 100 yields a 1`V signal to the ADC input.

U51 AD626AR

+5V unfiltered +2.5V_IN 5Vanalog

C119 100nF

Imon+2.5V

Assuming a 200 mW load on +2.5V, a gain of 100 yields a 400mV signal to the ADC input.

U45 AD626AR

+5V unfiltered +1.8V_IN 5Vanalog

JU7 Jumper

C120 100nF

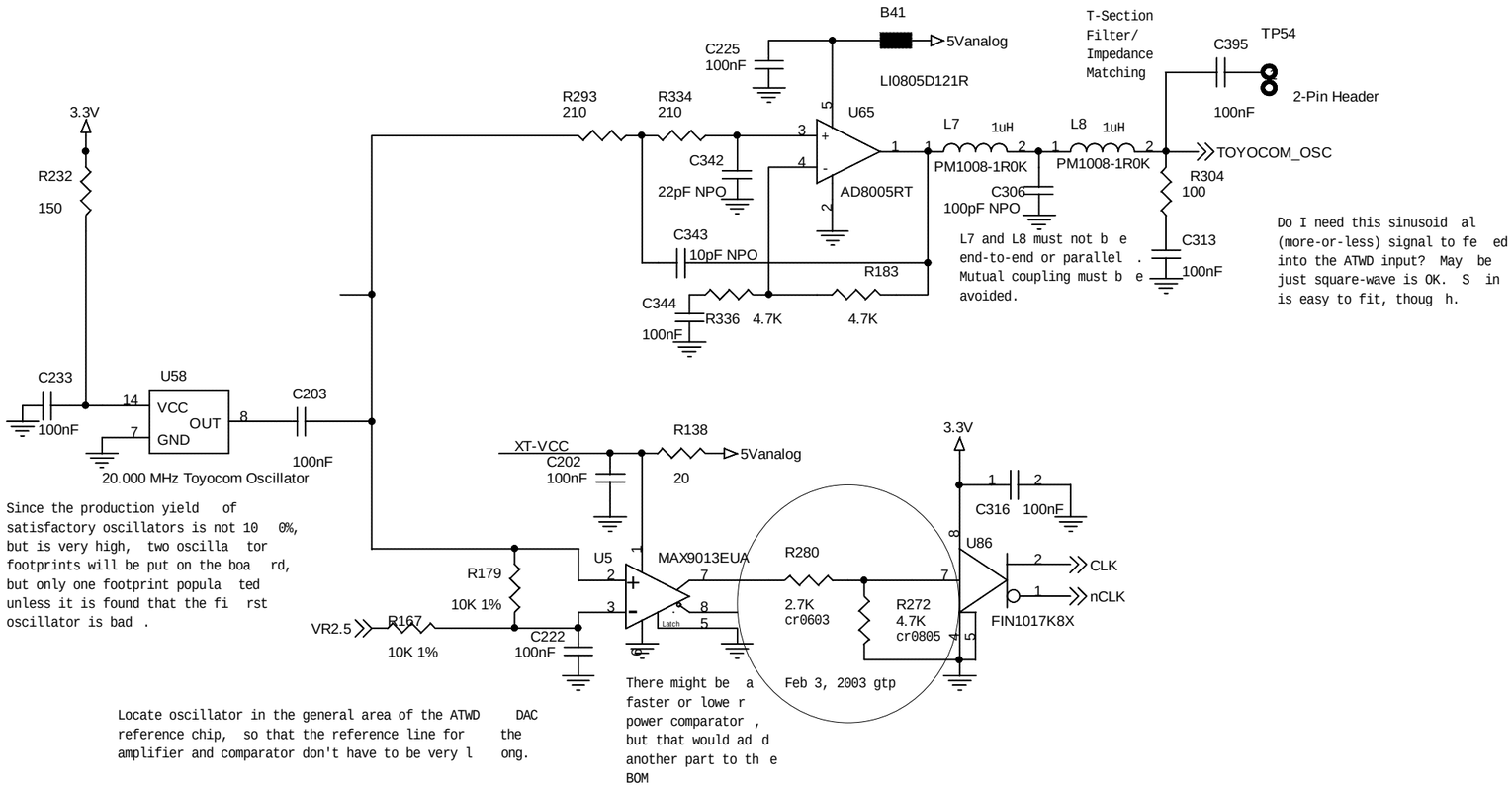
Imon+1.8V

Assuming a one Watt load on +1.8V, a gain of 10 yields a 200mV signal to the ADC input.

Title: Digital Optical Module Power Supply

Size: C | Document Number: <Doc> | Rev: <RevCode>

Date: Tuesday, March 11, 2003 | Sheet 14 of 15



Title	Digital Optical Module Crystal	
Size B	Document Number <Doc>	Rev <RevCode>
Date: Tuesday, March 11, 2003	Sheet 15 of 15	