Since the sensor u ses about 60mW, it would be p rudent to disable power to it when not needed.

It remains to be seen how prudent it is to f loat the ground lead. The alternative may be a P-FET in the Vcc enable d by the N-FET.

C75 1uF X7R
C82 10nF
U26
TP60 2-Pin Header
R338 24.9K 1%
R339 10K 1%
MPXA4115A
5Vanalog
BAROMETER
BAROMETER_ENA
Q7
R407 10K 1%
2N7002

Vout=Vs(0.009*P-0.09 5)+/-Error
P = 111.1111111*Vs*Vout +10.55555556
5V and Baro are scaled by the same factor, so are in the same units.

U67 MAX4166ESA
3.3V
R3 100K 1%
R1 100K 1%
R279 100K 1%
R11 61.9K 1%
R12 24.9K 1%
C1 100nF

-(-5/2.5)-(+3.3+2.5+1. 8)/4 =Vout
2 - 0.825 - 0.625 - 0.4 50) = 0.100V
Lets just assume tha t if +5 is gone, we're dead. T he 5V CPU supervisory chip input will cause reboot below about 4.750V.

R13
R4 10K 1%
24.9K 1%

Place resistors ne ar remote sources. Capacit ors near ADC.

BAROMETER
Imon+5V
Imon+3.3V
Imon+2.5V
Imon+1.8V
Imon-5V
R5 10K 1%
R6 10K 1%
R7 10K 1%
R8 10K 1%
R9 10K 1%
R10 10K 1%

U61 0-2.5V span
CH0 CH1 CH2 CH3 CH4 CH5 CH6 CH7
CS SCLK DIN DOUT STRB SHDN VDD VSS REFADJ VREF DGND AGND
ADC_nCS0 DAC_SCLK DAC_DIN ADC_DOUT
MAX146BEAP
(2.500/4096) x count
R367 20
3.3V
C14 2.2uF 6.3V Tan
C9 100nF
C10 100nF
C11 10uF 6.8V Tan
C2 C3 C4 C5 C6 C7 C8 100nF

Part values ending in "*" should not be mounted. These parts are for diagnostics or implementation of alternate methodologies.

TI claims to have a lowe r power part, but only accurate to 2 de g C (probably within the -25C and abo ve range)...

U55 DS1631U
TEMP_SENSOR_CLK
TEMP_SENSOR_IO
R51 10K 1%
3.3V

4.25 mW x 4 + 7.5mW = 24.5 mW
plus 3.3mW when converting temperature
+ 6mW x 10V/conv_ef f = 67 mW

If we can use the 2.5V reference output of the ADC, then we can ele iminate the TLE2425 reference chip.

U24 TLE2425ID
C12 100nF
JU26 Jumper
JU30 Open Ckt
TP1 TP*
U23 MAX5250BEAP
DAC_CS2 DAC_SCLK DAC_DIN DAC-DO0 DAC-UP0 DAC_CL COMREF_2.5
OUTA OUTB OUTC OUTD FBA FBB FBC FBD REFCD REFAB DGND AGND VDD CS SCLK DIN DOUT UPO PDL CL
DISC-MultiSPE DISC-OneSPE SingleLED-BRIGHTNESS-CTL 5V out put FADC_0_Ref
R14 R15 R16 R17 10K 1%
C13 100nF
C15 100nF
C270 OSCON_6SC6R8M

The (differential input) 4 0 MHz ADC non inverting input, used as th e center-scale reference.

A 10uF Tantalum capa citor is needed on U4-1 to insure stability. gtp 4/13/09

In the IceCube DOM, a surface mount part should rep lace this through-hole part

Components w hose value ends i n "*" are not to be mounted.

R36 100
FADC_0_Ref
C385 10uF 6.8V Tan
C386 100nF
R39 20

Note that this FADC is differ ential input. Amplifier and shaper stages are DC coupled. The 'bottom' of the span depends on the setting of the ATWD pedestal voltage. I.e., Pedestal for the FADC = Pedestal for the ATWD. V + in must be set to ( Vpedestal - (span/2) ) vol ts, or a few mV lower.

100 mW

U30 AD9215BRU-65
VIN+ VIN- REFT REFB VREF SENSE OTR CLK PDWN MODE DVdd AVdd AVdd DGnd AGnd AGnd D0 D1 D2 D3 D4 D5 D6 D7 D8 D9
FLASH_AD_D0 FLASH_AD_D1 FLASH_AD_D2 FLASH_AD_D3 FLASH_AD_D4 FLASH_AD_D5 FLASH_AD_D6 FLASH_AD_D7 FLASH_AD_D8 FLASH_AD_D9
R436 R437 R438 R439 R440 R441 R442 R443 R444 R445 100
FLASH_NCO
FLASH_AD_STBY
2.5V
3.3V
B18 LI08050121R
FADC_In
R132 20
C26 10uF 6.8V Tan
C125 100nF
C126 100nF
C124 100nF
C29 C127 100nF
ADC-REF
C294 10uF 6.8V Tan
C295 100nF
JU28 Open Ckt
JU27 Jumper
R45 Open Ckt Ra*
R46 Open Ckt Ra*

Jumpers and RC netwo rk close to U30

JU29 Open Ckt
JU21 Jumper
CLKx2
FLASH_AD_CLK
R2 51
C121 100pF NPO

Strap SENSE to Gnd f or 2V Span.
Strap SENSE to VREF f or 1V span.
Strap SENSE to Voltage Di vider for span =1.0(1+Ra/ Rb).

U28 MAX5250BEAP 10 bit DAC
DAC_CS3 DAC_SCLK DAC_DIN DAC-DO1 DAC-UP1 DAC_CL
TP2 TP*
FE_TEST_PULSE_AMPL Clamp DAC_Out_0 DAC_Out_1
R22 R23 R24 R25 10K 0.1%
C16 100nF
C17 100nF
R26 R27 R28 R29 10K 0.1%

U73 MAX534BEEE 8 bit DAC
DAC_CS4 DAC_SCLK DAC_DIN DAC-DO2 DAC-UP2 DAC_CL
TP3 TP*
Spare_8bit_DAC_0 Spare_8bit_DAC_1 Spare_8bit_DAC_2 Spare_8bit_DAC_3
Vout=(Vref* n/256)
5Vanalog R262 1K 1%
C272 100nF
C271 OSCON_6SC6R8M
C273 100nF

R55 20*
3.3V
C418 100nF*
U79 LTC1594IS*
ADC_IN0 ADC_IN1 ADC_IN2 ADC_IN3
R446 R447 R448 R449 10K 1%*
In0 In1 In2 In3 MuxOut ADC_In Vref Com Gnd Vdd Vdd CLK DIN MUX_CS ADC_CS ADC_DOut
DAC_SCLK DAC_DIN
MUX_nCS0 ADC_nCS1 ADC_DOUT
ADC_COM
JU31 Jumper
COMREF_2.5
C423 100nF*
R63 Jumper
C419 C420 C421 C422 100nF*

To be used to control and read out an alternate hig h voltage power supply, if such a course is taken.

| | | | |
|---|---|---|---|
| Title | Digital Optical Module AD/DA | | |
| Size C | Document Number <Doc> | | Rev 1.1 |
| Date: Wednesday, October 09, 2002 | Sheet 3 | of 14 | |

Per criterion established July 2002 (gtp&drn) the design goal for the IceCube DOM is 200 PE = 1V into the ATWD dic tated by PMT saturation behavior. Namely, the PMT NEVER delivers mor e than about 2V, and is linear to about 1V into a 50 ohm load (100 oh m || back-termination).

Locate these amplifiers --> close to the PMT signal input.

1*1.3*5 + 2*1.3*5 + 6.8*10 + 2* 1.15*10+2*1.1*5+ 3*0.4*10=13 4 mW
opamp comparator, 1135 80 14 8014 8005

AD advertises that these (400 MHz) amplifiers re cover in 60 ns. At 5 mW per stage, they give slightly less performance than an HA1135 at 1/10th the current. Saturation is not a big issue for t he (latching) comparator input, since latch recovery is contr olled by the FPGA

If we have power to burn, once all revisions are taken into account, the 850 MHz bandwidth HA1135 may prove to be a bett er choice as comparator input amplifier, as one stage should hav e less delay than 2.

The comparators exhibit less trigger delay i f driven by a positive signal, so the second gain stage inverts. The first one buffers to minimize load on the PMT signal.

If test pulser, U52, injects too much power supply noise, it will have to go, in favor of something that is quieter.

Calibration input test-point. Drive with 5V square wave to generate fixed amplitude test pulses.

Caution: The comparato rs are 5V parts that cannot be ope rated from 3.3V. Care must be taken to protect the driven 3.3V part.

Delay Line Subassembly

Test pulse inj ection (if it doesn't work, remove transf ormer, and use jum per.)

If the PMT delivers 3V into a 50 ohm load, then change the divider resistors to R30=16.8, a nd R54=66.5 Leave the gain of the amplifier unchanged. The design goal is to have the PMT saturation volta ge within the span of the ATWD.

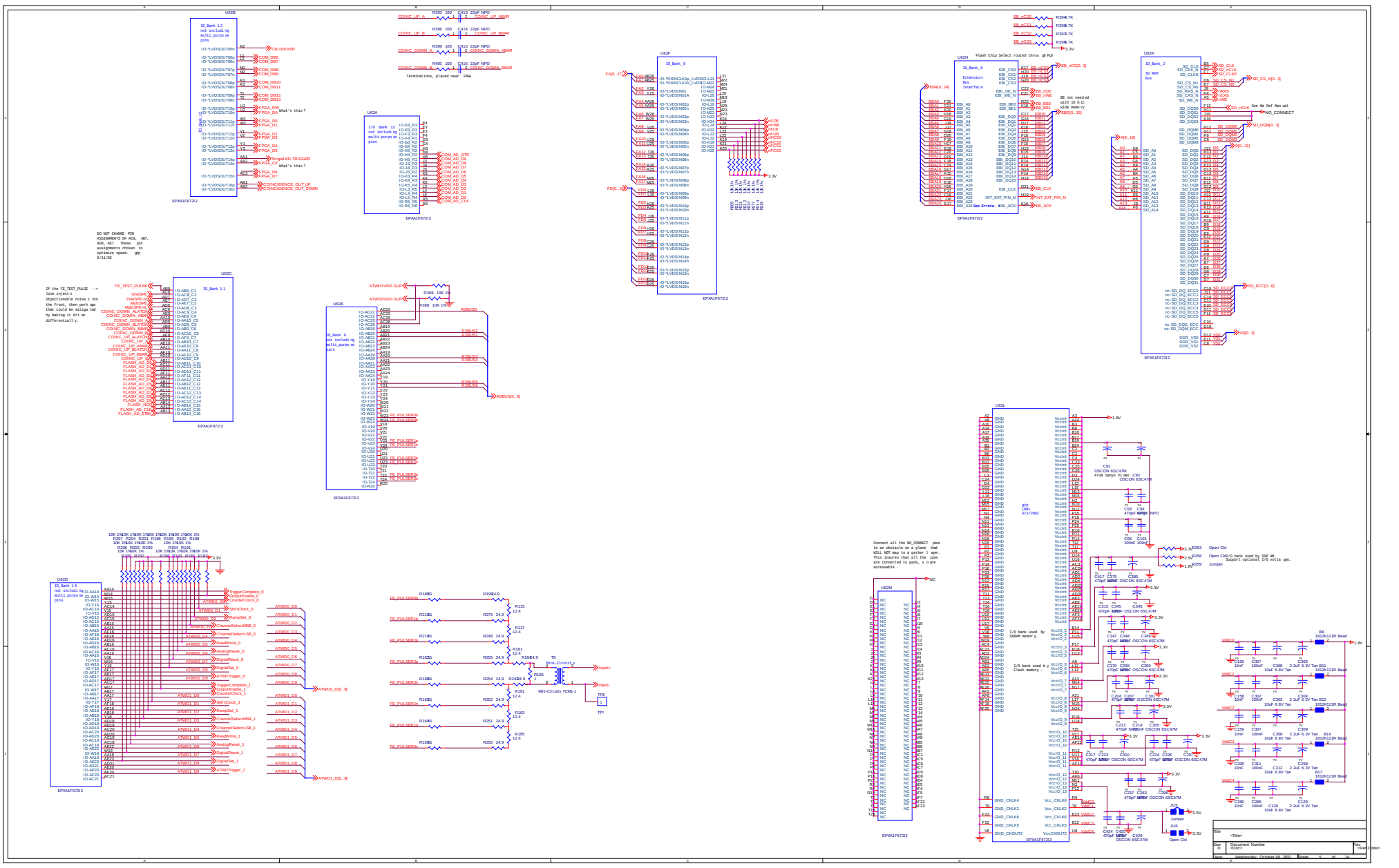
0.47uF Y5V
Samsung CL31F4 74ZBNC
(0.12)

Should the A DC channel be DC coupled?

optimized for 200 MHz BW
Also try observi ng the performance of this stage with 499 a nd 249 ohm feedback div ider. See if it is st ill as stable. It shoul d have more bandwi dth.

The shaped signal path design was from Harold Yaver of the Engineering Department.
-Modifications added to insure stable offset behavior, and to offset the output to match the input range of the ADC

| | | | |
|---|---|---|---|
| Lawrence Berkeley National Laboratory | | | GTP/JL/DRN/HY |
| Title: Digital Optical Module Analog Front End | | | |
| Size: C | Document Number: <Doc> | | Rev: 0 |
| Date: Wednesday, October 09, 2002 | | Sheet 4 of 14 | |


U62B
U62A
U62E
U62C
U62F
U62H
U62K
U62L
U62M
U62D
EPXA1F672I2
EPXA1F7202
DO NOT CHANGE PIN ASSIGNMENTS OF ACB, ADT, ADB, AET. These pin assignments chosen to optimize speed. gtp 5/11/02
If the FE_TEST_PULSE --> line inject s objectionable noise i nto the front, then perh aps that could be mitiga ted by making it dri ve differentially.
Flash Chip Select routed throu gh PLD
BE not needed with 16 b it wide memory
Connect all the NO_CONNECT pins to an obstacle on a plane that WILL NOT map to a gerber l ayer. This insures that all the pins are connected to pads, s o are accessable.
I/O bank used by 3.3V Flash memory .
I/O bank used by 1.8V memor y.
Open Ckt
Open Ckt/0 bank used by 32K 4K, Support optional I/O volta ges.
Jumper
Mini-Circuits TCM1-1
Title
<Title>
Document Number
<Doc>
Rev
<Rev Code>
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Multiplexed Calibration In puts:
Trackme Gus for capture rate calibration, and absolute ph ase reference
Clk Osc 40 MHz system clock
Flash current waveform For LED on DOM M ain Board
Flash current waveform for LED daught er board
Local Coincidence Signal from upper neighbor
Local Coincidence Signal from lower neighbor
Communications Signal for relative phase of time ticks
Communications Signal for relative phase of time ticks

For best integrity of calibration, mount the two MAX141 chips such that the 20 ohm resisto r outputs abut, and pin 11 to the 20 ohm resistor is the same length, and leads to inputs are kept short s inas they are high frequency carri ers.

If noise is being coupled throug h, then put a resistor or be ad here.

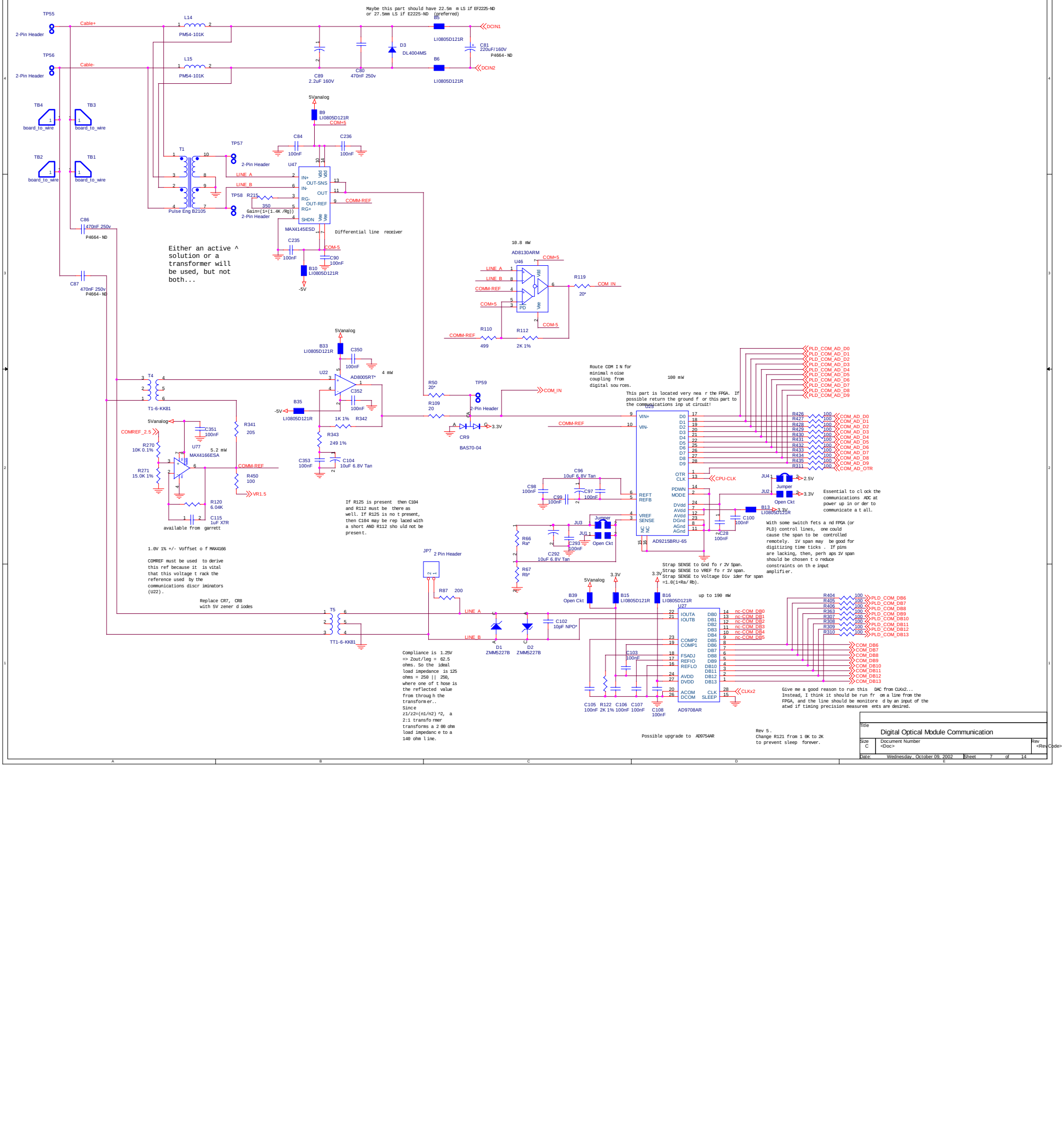
Power Budg et:
50 + 50 + 1 + 5.1 + 5.1 + 4.25 + 4.25 + 2xMAX mW

Could be a lower power part with greater delay, like max999, if it is ne cessary to save 6mW .

Use a low volta ge driving standard. Wi red to a low voltage I /O bank of the FP GA

SEMICONWELL 2964-2966 S cott Blvd. Santa Clara, CA 9 5054 Tel:(408)986-80 26 Fax:(408)-850-1101, or equivalent .

| | | |
|---|---|---|
| Title | Digital Optical Module ATWD | |
| Size: D | Document Number <Doc> | Rev <Revision Code> |
| Date: Wednesday, October 09, 2002 | Sheet 6 of 14 | |


Maybe this part should have 22.5m m LS if EF2225-ND
or 27.5mm LS if E2225-ND (preferred)
TP55
Cable+
2-Pin Header
TP56
Cable-
2-Pin Header
L14
PM54-101K
L15
PM54-101K
B5
LI0805D121R
B6
LI0805D121R
DCIN1
DCIN2
C89
2.2uF 160V
C80
470nF 250v
D3
DL4004MS
C81
220uF/160V
P4664-ND
TB4
board_to_wire
TB3
board_to_wire
TB2
board_to_wire
TB1
board_to_wire
T1
Pulse Eng B2105
5Vanalog
B9
LI0805D121R
COM+5
C84
100nF
C236
100nF
TP57
2-Pin Header
U47
MAX4145ESD
IN+
IN-
RG-
RG+
SHDN
OUT-SNS
OUT
OUT-REF
Vdd
Vee
LINE_A
LINE_B
TP58
R215
350
Gain=(1+(1.4K /Rg))
2-Pin Header
COMM-REF
Differential line receiver
C235
100nF
C90
100nF
COM-5
B10
LI0805D121R
-5V
C86
470nF 250v
P4664-ND
C87
470nF 250v
P4664-ND
Either an active ^
solution or a
transformer will
be used, but not
both...
10.8 mW
AD8130ARM
U46
LINE_A
LINE_B
COMM-REF
COM+5
PD
R119
20*
COM_IN
R110
499
R112
2K 1%
T4
T1-6-KK81
5Vanalog
B33
LI0805D121R
C350
100nF
U22
AD8005RT*
4 mW
C352
100nF
B35
LI0805D121R
-5V
1K 1%
R342
R343
249 1%
C353
100nF
C104
10uF 6.8V Tan
R50
20*
R109
20
TP59
2-Pin Header
COM_IN
CR9
BAS70-04
3.3V
Route COM I N for
minimal noise
coupling from
digital sou rces.
100 mW
This part is located very nea r the FPGA. If
possible return the ground f or this part to
the communications inp ut circuit!
PLD_COM_AD_D0
PLD_COM_AD_D1
PLD_COM_AD_D2
PLD_COM_AD_D3
PLD_COM_AD_D4
PLD_COM_AD_D5
PLD_COM_AD_D6
PLD_COM_AD_D7
PLD_COM_AD_D8
PLD_COM_AD_D9
R426 100
R427 100
R428 100
R429 100
R430 100
R431 100
R432 100
R433 100
R434 100
R435 100
R311 100
COM_AD_D0
COM_AD_D1
COM_AD_D2
COM_AD_D3
COM_AD_D4
COM_AD_D5
COM_AD_D6
COM_AD_D7
COM_AD_D8
COM_AD_D9
COM_AD_OTR
U25
AD9215BRU-65
VIN+
VIN-
REFT
REFB
VREF
SENSE
PDWN
MODE
OTR
CLK
DVdd
AVdd
AVdd
DGnd
AGnd
AGnd
CPU-CLK
C96
10uF 6.8V Tan
C98
100nF
C99
100nF
C97
100nF
JU4
JU2
Jumper
2.5V
3.3V
Open Ckt
B13
LI0805D121R
3.3V
C100
100nF
C28
100nF
Essential to cl ock the
communications ADC at
power up in or der to
communicate a t all.
With some switch fets a nd FPGA (or
PLD) control lines, one could
cause the span to be controlled
remotely. 1V span may be good for
digitizing time ticks . If pins
are lacking, then, perh aps 1V span
should be chosen t o reduce
constraints on th e input
amplifier.
JU3
Jumper
JU1
Open Ckt
C293
100nF
C292
10uF 6.8V Tan
R66
Ra*
R67
Rb*
Strap SENSE to Gnd fo r 2V Span.
Strap SENSE to VREF fo r 1V span.
Strap SENSE to Voltage Div ider for span
=1.0(1+Ra/Rb).
COMREF_2.5
R270
10K 0.1%
R271
15.0K 1%
U77
MAX4166ESA
5.2 mW
C351
100nF
R341
205
COMM-REF
R450
100
VR1.5
R120
6.04K
C115
1uF X7R
available from garrett
1.0V 1% +/- Voffset o f MAX4166
COMREF must be used to derive
this ref because it is vital
that this voltage t rack the
reference used by the
communications discr iminators
(U22).
If R125 is present then C104
and R112 must be there as
well. If R125 is no t present,
then C104 may be rep laced with
a short AND R112 sho uld not be
present.
Replace CR7, CR8
with 5V zener d iodes
JP7
2 Pin Header
R87 200
T5
TT1-6-KK81
LINE_A
LINE_B
D1
ZMM5227B
D2
ZMM5227B
C102
10pF NPO*
Compliance is 1.25V
=> Zout/leg = 62.5
ohms. So the ideal
load impedance is 125
ohms = 250 || 250,
where one of t hose is
the reflected value
from throug h the
transform er..
Since
z1/z2=(n1/n2) ^2, a
2:1 transfo rmer
transforms a 2 00 ohm
load impedanc e to a
140 ohm line.
5Vanalog
3.3V
3.3V
B39
Open Ckt
B15
LI0805D121R
B16
LI0805D121R
up to 190 mW
U27
AD9708AR
IOUTA
IOUTB
COMP2
COMP1
FSADJ
REFIO
REFLO
AVDD
DVDD
ACOM
DCOM
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
DB8
DB9
DB10
DB11
DB12
DB13
CLK
SLEEP
nc-COM_DB0
nc-COM_DB1
nc-COM_DB2
nc-COM_DB3
nc-COM_DB4
nc-COM_DB5
CLKx2
C103
100nF
C105
100nF
R122
2K 1%
C106
100nF
C107
100nF
C108
100nF
R404 100
R405 100
R406 100
R363 100
R307 100
R308 100
R309 100
R310 100
PLD_COM_DB6
PLD_COM_DB7
PLD_COM_DB8
PLD_COM_DB9
PLD_COM_DB10
PLD_COM_DB11
PLD_COM_DB12
PLD_COM_DB13
COM_DB6
COM_DB7
COM_DB8
COM_DB9
COM_DB10
COM_DB11
COM_DB12
COM_DB13
Give me a good reason to run this DAC from CLKx2...
Instead, I think it should be run fr om a line from the
FPGA, and the line should be monitore d by an input of the
atwd if timing precision measurem ents are desired.
Possible upgrade to AD9754AR
Rev 5.
Change R121 from 1 0K to 2K
to prevent sleep forever.
Title
Digital Optical Module Communication
Size C
Document Number
<Doc>
Rev
<Rev Code>
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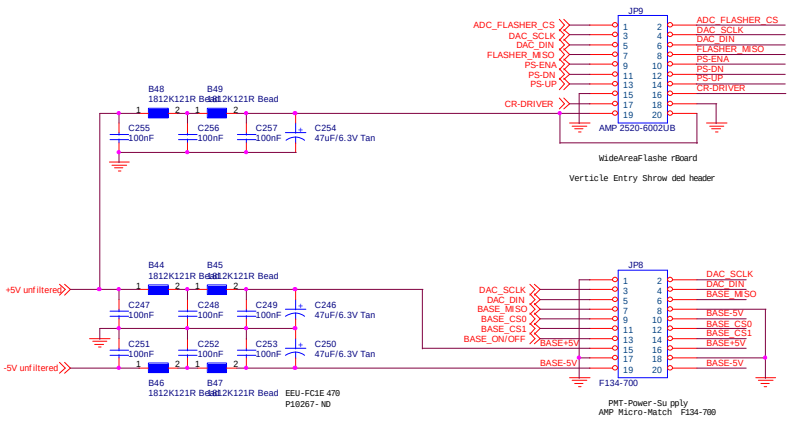
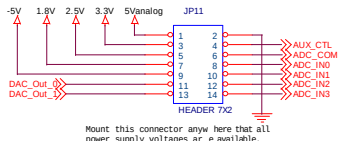
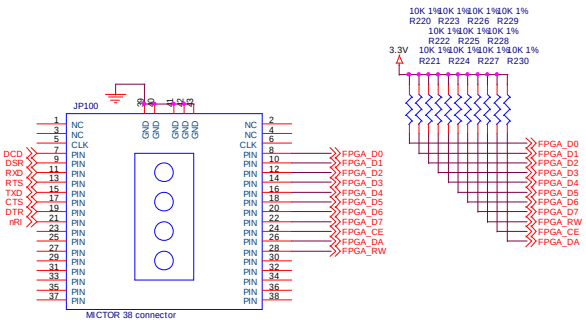



1 GND
2 SCK - Serial clock
3 SCK
4 MOSI -Serial data in
5 MOSI
6 MISO - Serial d ata out
7 MISO
8 GND
9 CS0 (DAC) - Chip sele ct for DAC
10 CS0
11 CS1 (ADC) - Chip sel ect for ADC
12 CS1
13 ON/OFF - Power supply e nable/disable
14 ON/OFF
15 +5V - Main power
16 +5V
17 GND
18 GND
19 -5V - Main power
20 -5V

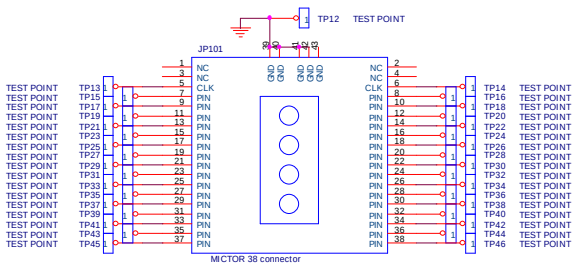



Mount this connector anyw here that all power supply voltages ar e available.

Can be used to power and control altern ate PMT power supply




Compatible with model P6434 probe for Tektronix logic analyzer.




This connector is meant to be used dur ing pre-production debugging. The footpring should be mounted on a part of the board that is later broken off and discarded. T he test-points will be used to tack down one of wires that bring s ignals out of the main board.

Compatible with model P6434 probe for Tektronix logic analyzer.

| | | | |
|---|---|---|---|
| Title | Off-Board Subsystems | | |
| Size C | Document Number <Doc> | | Rev <RevCode> |
| Date: Wednesday, October 09, 2002 | | Sheet 8 of 14 | |

Design for 1V output swing of driver=>0.5V at port =>0.3535V at sum port.
0.3535V from neighbor at sum port => 0.175V at port B => 0.87V threshold.
Tune with resistor between bases of Q21, Q22.

Drive this node with Tri-State output of FPGA.
A pull-up will deliver a positive unit pulse.
A pull-down will deliver a negative unit pulse.

Balanced output to minimise noise on the board during an event.

Note to FPGA designer:
'COINCIDENCE_OUT_Nxx lines must 'float' when not signaling (ie high-Z state of tri-state output). Both positive and negative pulses are permitted by pulling up or down on the inputs to the driver op-amps.

COINCIDENCE_OUT_UP
COINCIDENCE_OUT_DOWN
COINC_REF

5Vanalog
3.3V

B20 LI0805D121R
B36 LI0805D121R
B21 LI0805D121R
B7 LI0805D121R
B37 LI0805D121R
B40 LI0805D121R

C160 100nF
C387 100nF
C162 100nF
C59 100nF
C390100nF
C62 100nF

R141 1.1K
R374 1.1K
R139 499
R377 499
R372 1K 1%
R144 1K 1%
R143 75.0
R376 75.0
R379 1K 1%
R380 1K 1%
R373 15.0K 1%
R375 1K 1%
R378 1K 1%
R381 15.0K 1%
R383 100
R382 8.1K

U40 AD8005RT
U59 AD8005RT
U64 MAX4166ESA
U6 MAX9013EUA
U7 MAX9013EUA
U8 MAX9013EUA
U9 MAX9013EUA

Thresholds should be +/- 0.08V or so above and below COINC_REF.

C389 100nF
C388 1uF X7R

I good four quadrent low power 1.65V reverence could be used in place of the MAX4166 and associated circuitry. A potential problem for this circuit is the stability of the MAX4161 when either or both of the opamps are driven. Varify with first prototype.

TP47 2-Pin Header
TP48 2-Pin Header
TP49 2-Pin Header
TP50 2-Pin Header
TP51 2-Pin Header
TP52 2-Pin Header

LOCAL_COINCIDENCE_Upper
LOCAL_COINCIDENCE_Lower

R145 2.2K
R146 2.2K
R385 2.2K
R386 2.2K
C163 47pF NPO
C164 47pF NPO
C391 147pF NPO
C392 47pF NPO

COINC_UP_ALATCH
COINC_UP_BLATCH
COINC_DOWN_ALATCH
COINC_DOWN_BLATCH

U11 FSTD3125M
U10 FSTD3125M

R360 51
R359 51
R357 51
R358 51
R356 51
R350 51
R345 51
R347 51

COINC_UP_ABAR
COINC_UP_A
COINC_UP_B
COINC_UP_BBAR
COINC_DOWN_ABAR
COINC_DOWN_A
COINC_DOWN_B
COINC_DOWN_BBAR

TB5 board_to_wire
TB6 board_to_wire
TB7 board_to_wire
TB8 board_to_wire

T3 T2 T3-1T-K81

sum_up
sum_down
port_1up
port_1down
port_2up
port_2down
Coincidence-REF

Z1A PSC-2-2-75
Z2A PSC-2-2-75

SUM PORT
GROUND
PORT 1
PORT 2

A balanced waveform, like AMI, is desirable for transmission over this pathway.

CAUTION
Gnd of PSC-2-2 operates at pedestal potential

It may be possible to replace the PSC-2-2 with a simple transformer, but this requires taking into account impedance matching side-effects. In any case, T2, T3 will have to be chosen to match the splitter to the twisted pair cable.

C393 1nF NPO
C394 10nF
C165 100nF

Make sure that when the op-amps are driven, there is no significant bounce on the 'ground' pins of the power splitters.

R125 150*
R137 150*
Z2B T1-6-KK81*
Z1B T1-6-KK81*

Power = 4*1.3*5 + 2*0.4*5 + 1*1.3*5 = 36 mW

Title: Digital Optical Module Local Coincidence
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Flash Chip Select routed through PLD

60mA x 2.5V = 150 mW per memory chip

To provide the compatibility with the AMD Am29DL 322D

4 Megabyte Flash Memory

With the PLD using a driver, I don't think these pull-ups are needed.

AMD Memory requires a +12V programming voltage

Samsung 8 Megabyte 32 bit wide memory for mobile computers (laptop) has reasonable power. Several of their products have the same footprint.
K4S64323LF-S( D)U15 (superlow power -25C)
K4S64323LF-S( D)P15 (low power - 40C)
2.5V core, 1.8V I/O.
1.8V I/O requires special register set-up for CPU.

Power: 3.3V * 75mA for SELECTED chip = 247.5 mW

Title: Digital Optical Module Memory

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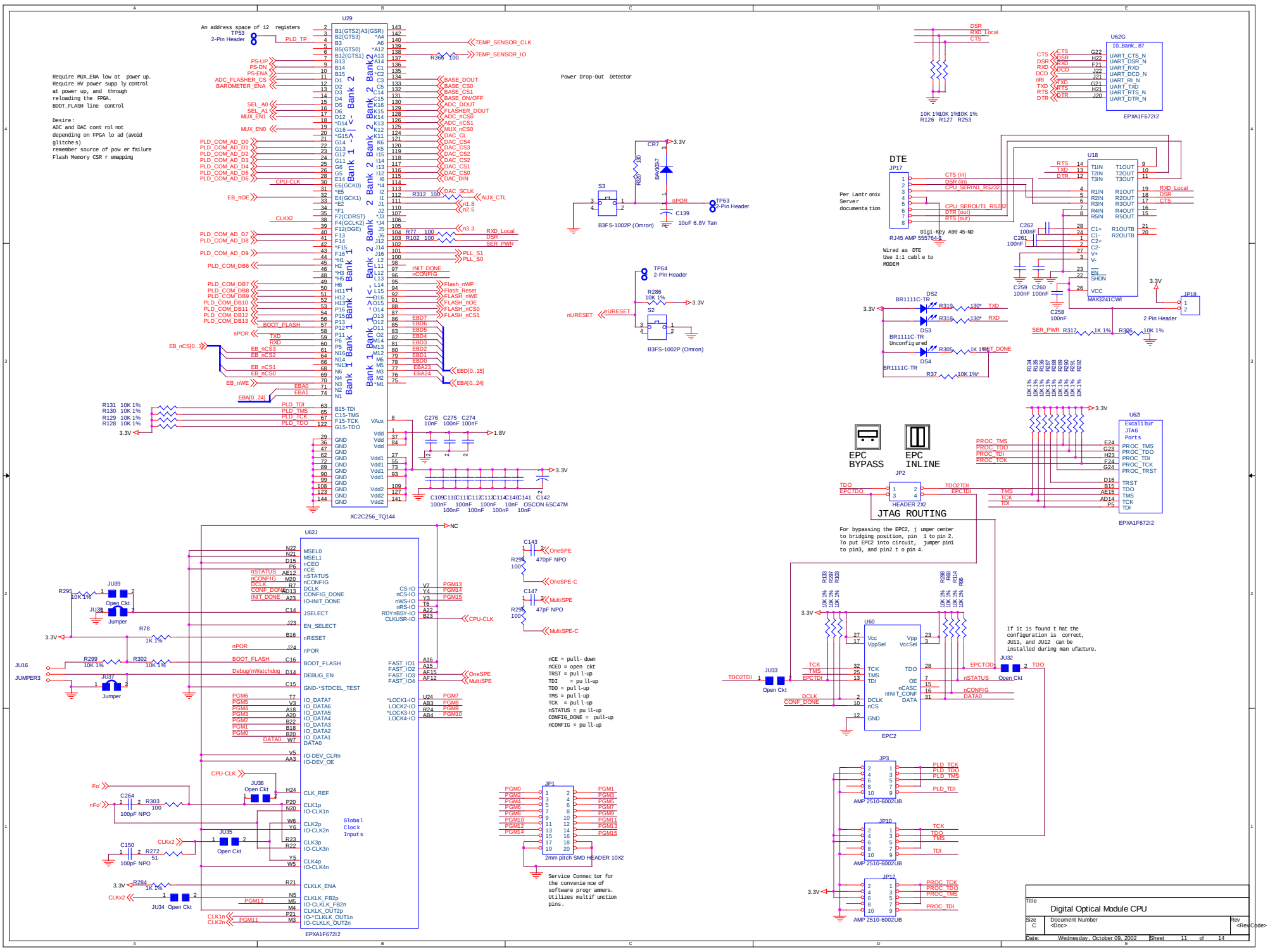
Require MUX_ENA low at power up.
Require HV power supp ly control at power up, and through reloading the FPGA.
BOOT_FLASH line control
Desire:
ADC and DAC cont rol not depending on FPGA lo ad (avoid glitches)
remember source of pow er failure
Flash Memory CSR r emapping
An address space of 12 registers
U29
XC2C256_TQ144
Power Drop-Out Detector
CR7
BAV103
B3FS-1002P (Omron)
TP64
2-Pin Header
DTE
JP17
RJ45 AMP 555764-1
Digi-Key A90 45-ND
Per Lantronix Server documentation
Wired as DTE
Use 1:1 cable to MODEM
U18
MAX3241CWI
DS2
DS3
DS4
BR1111C-TR
Unconfigured
JP18
2 Pin Header
EPC BYPASS
EPC INLINE
JP2
HEADER 2X2
JTAG ROUTING
For bypassing the EPC2, jumper center to bridging position, pin 1 to pin 2.
To put EPC2 into circuit, jumper pins 2 to pin3, and pin2 to pin 4.
U62I
Excalibur JTAG Ports
EPXA1F672I2
U62G
IO_Bank_B7
EPXA1F672I2
U62J
EPXA1F672I2
JU39
JU38
JU37
JU36
JU35
JU34
JU33
JU32
Open Ckt
Jumper
JUMPER3
U60
EPC2
nCE = pull- down
nCEO = open ckt
TRST = pul l-up
TDI = pu ll-up
TDO = pul l-up
TMS = pul l-up
TCK = pul l-up
nSTATUS = pu ll-up
CONFIG_DONE = pull-up
nCONFIG = pu ll-up
If it is found t hat the configuration is correct, JU31, and JU32 can be installed during man ufacture.
JP1
2mm pitch SMD HEADER 10X2
Service Connec tor for the convenie nce of software progr ammers. Utilizes multif unction pins.
JP3
JP10
JP12
AMP 2510-6002UB
Digital Optical Module CPU
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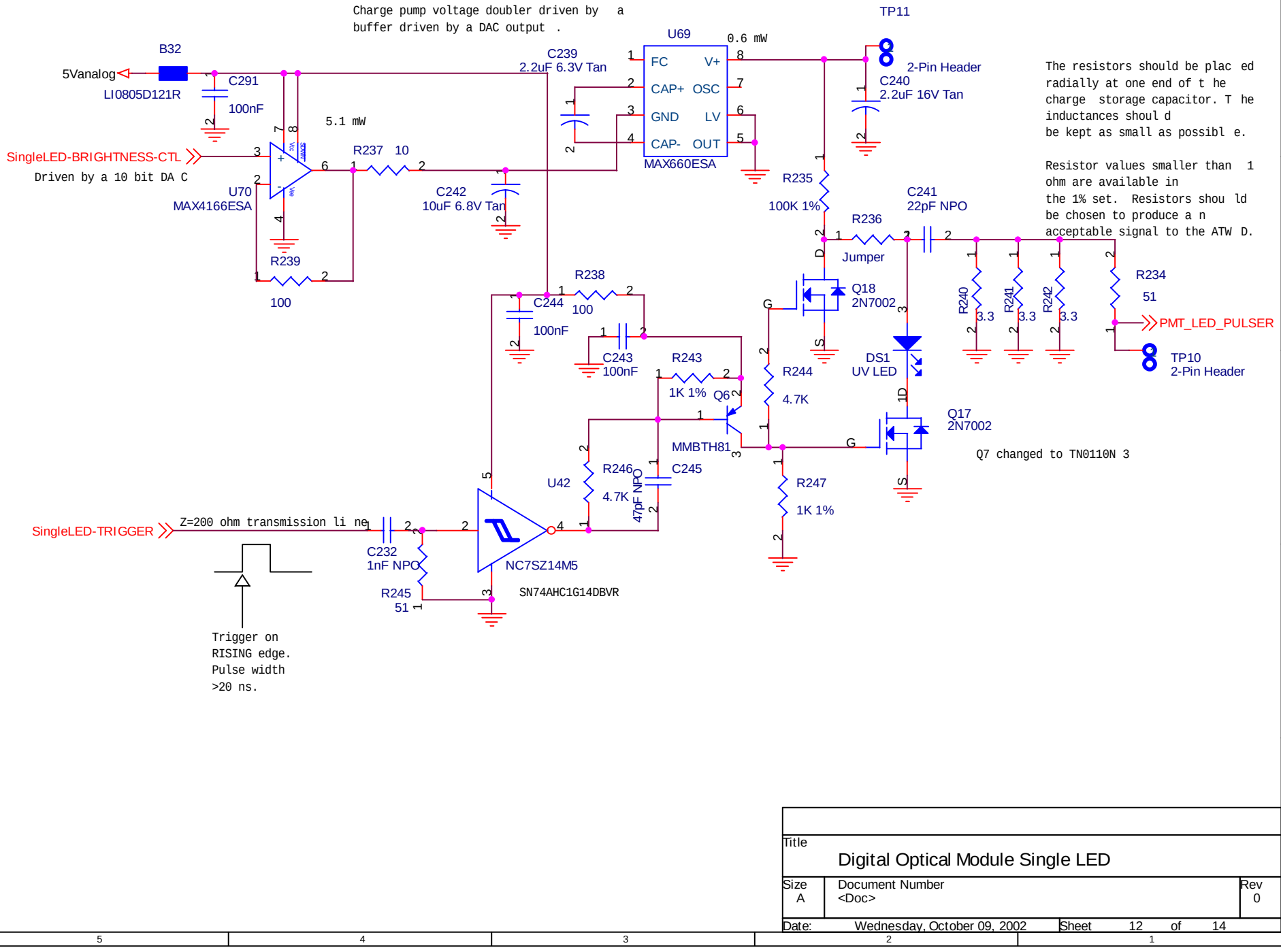


| | | |
|---|---|---|
| Title | Digital Optical Module Single LED | |
| Size A | Document Number <Doc> | Rev 0 |
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Over-Voltage protection f or the power supply. I suppose, th is could as easily be balanced, using just the N and P FETs. If it is dee med that the power supply input vol tage range (and tolerence) is great enough, the protection circuit can be deleted from the des ign.

Digi-Key Panasonic PK1064-N D ELF-15N002A

DCIN1 / DCIN2 — B22 1812K121R Bead, L10, C407 100nF, B26 1812K121R Bead, ELF-15N002A

BZX84C6V8DI CT-ND — CR4 CMHZ5263B, CR5 CMHZ5263B, R315 10M, R316 10K 1%, Q13 TN2510N8 Supertex, Q19 2N7002, CR2 CMHZ5235B

<-- 112V -->

C85 2.2uF 160V, C178 470nF 250v, L13 2.2mH API 2474 series, L14 2.2mH API 2474 series, C88 2.2uF 160V, C375 470nF 250v, C179 470nF 250v, B23 1812K121R Bead, B27 1812K121R Bead

NOVAcap 1812Z474M2 5INX 250V Z5U Ceramic Capacit or

PS1 — 70 IMX 4-0505-9 Power-One (40-120V, Vin+, Vin-, +5V, COM, -5V)

The Ericsson power supp ly does not meet the new input voltage requirement for operation at 90 to 10 0V. It will be replaced with a suitab le product. Candidates are a 4 watt p roduct from Power-One (Melcher), an d a 7 watt product from Power-On e. Still searching for the best pro duct Sep 21, 2002 gt p.

+5V unf iltered — R285 0.100 — B24 1812K121R Bead, B25 1812K121R Bead, 5Vanalog, C180 100nF, C181 100nF, C182 100nF, C234 47uF/6.3V Tan, C238 47uF/6.3V Tan, EEU-FC1E 470 P10267-ND

-5V_supply — R151 0.100 — B28 1812K121R Bead, B29 1812K121R Bead, C183 100nF, C184 100nF, C185 100nF, -5V, EEU-FC1 E470 P10267-ND

-5V unf iltered

JP15 HEADER 4X2* (c0–c3)

For developm ent: A daughter card plugged into JP15 can be used to design an appr opriate filter net work.

U56 MAX1702BEGX

C187 OSCON_6SC6R8M +3.3V_IN — R116 0.100 — C190 100nF, C195 OSCON_6SC6R8M +2.5V_IN — R283 0.100 — C198 100nF, C398 OSCON_6SC6R8M +1.8V_IN — R282 0.100 — C403 100nF

+5V unf iltered

C221 OSCON_6SC6R8M +5V unfiltered — R389 100K 1%

R160 100K 1%, R158 Open Ckt, R153 100K 1%, R154 100K 1%, R155 100K 1%

OUT1

PS_nPOR, nURESET — Alternet power down-re set option.

INP1, INP2, INP3, Vdd, DBI, LBI, LBO, RSO, OUTOK, QN2, MR, PGM3, REF, LX1, OUT1, COMP1, LX2, FB2, COMP2, LX3, OUT3, COMP3

L2 PM105-100M 10uH, C186 OSCON_6SC6R8M, OUT1, C366 100nF, R157 33K, C191 33pF NPO, C193 1nF NPO

L9 PM54-100M 10uH, B31 1812K121R Bead, C362 100nF, C189 100nF, C364 47uF/6.3V Tan, C196 100nF — 3.3V

Switching inducto r could possibly be 4.7uH . Need at least 1.5 A max c urrent. Note that perme ability decreases a t low temperatur e...

L3 PM105-100M 10uH, C194 OSCON_6SC6R8M, R159 38.3K 1%, C367 100nF, R388 15.0K 1%, C363 100nF, L6 PM105-100M 10uH, B34 1812K121R Bead, C197 100nF, C365 47uF/6.3V Tan, C402 100nF, C188 100nF — 2.5V

R152 18K, C404 33pF NPO, C201 680pF NPO

L4 PM105-100M 10uH, C396 OSCON_6SC6R8M, C399 100nF, L1 PM105-100M 10uH, B38 1812K121R Bead, C401 100nF, C397 47uF/6.3V Tan, C200 100nF, C192 100nF — 1.8V, C404 100nF

R156 22K, C199 33pF NPO, C406 1nF NPO, C405 100nF

U39 — -5V unfiltered, -5V_supply, 5Vanalog, C118 100nF, +IN, -IN, OUT, FIL G100, +VS, -VS, AGND, AD626AR — Imon-5V

Assuming a 500 mW load on -5V, a gain of 100 yield s a 1V signal to t he ADC input .

U49 — +5V unfiltered, +5V, 5Vanalog, C116 100nF, AD626AR — Imon+5V

Assuming a 200 mW load on +5 V, a gain of 100 yields a 400mV sig nal to the ADC in put.

U50 — +5V unfiltered, +3.3V_IN, 5Vanalog, C117 100nF, AD626AR — Imon+3.3V

Assuming a 500 mW load on +3. 3V, a gain of 100 yields a 1 V sign al to the ADC in put.

U51 — +5V unfiltered, +2.5V_IN, 5Vanalog, C119 100nF, AD626AR — Imon+2.5V

Assuming a 2 00 mW load on +2.5 V, a gain of 100 y ields a 400mV sign al to the ADC in put.

U45 — +5V unfiltered, +1.8V_IN, 5Vanalog, C120 100nF, AD626AR — Imon+1.8V

Assuming a one Watt load on +1.8V, a gain of 10 yields a 200mV sig nal to the ADC i nput.

The MAX1702 contains voltage monitoring circuitry, and staged start circuitry that might make the volt age monitor chip, the LTC1727, unnecessary. However, the LTC1 727 provides outputs which can provide diagnostic inform ation to the PLD.

U78 LTC1727EMS8-2.5 — 3.3V, 2.5V, 1.8V, R85 68.1K 1%, R86 100K 1%, V3.3, V2.5, Vcca, Comp_3.3, Comp_2.5, RST, Comp_A

R98 100K 1%, R281 100K 1%, R97 10K 1%, R280 100K 1% — 3.3V

n3.3, n2.5, n1.8

JU10 Jumper — nPOR

JU9 Open Ckt — PS_nPOR

OSCON_6SC6R8M C321, C427, C339, C337, C335 — 5Vanalog

C322, C324, C326, C328, C330 — 100nF

C333, C331, C329, C327, C325 — -5V

C332, C334, C336, C338, C340 — 100nF

Distribute widely around th e PC board to improve noise suppression. If noise performance is good enough, some of these parts may be deleted from the final design. The design might benefit b y additional bypassing on 3.3V.

Title: Digital Optical Module Power Supply

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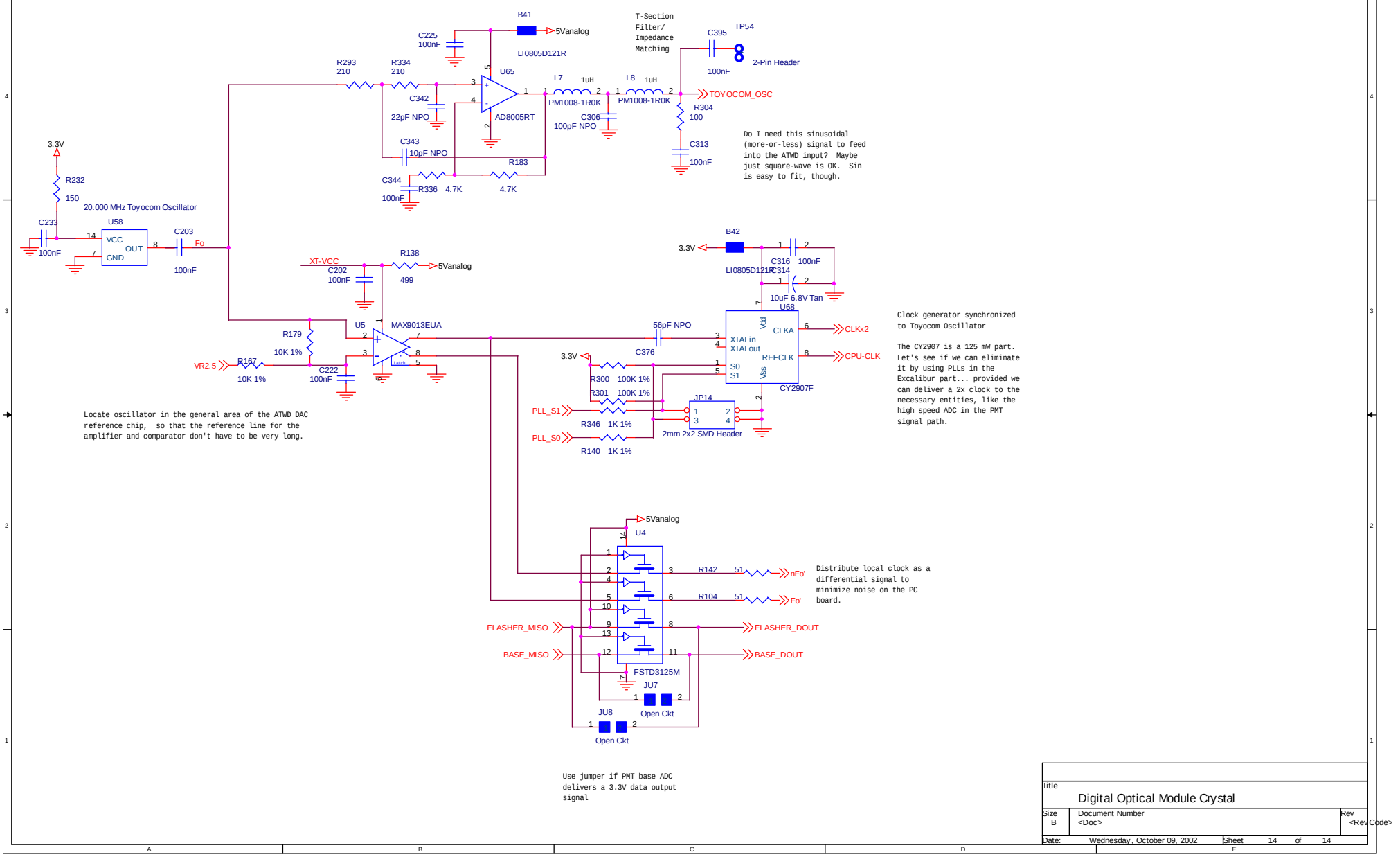


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|---|---|---|---|
| Title | Digital Optical Module Crystal | | |
| Size B | Document Number <Doc> | | Rev <RevCode> |
| Date: Wednesday, October 09, 2002 | | Sheet 14 of 14 | |