Board Stack-up:
TOP- Routing- Flud with ground plane where possible
Prepreg
INNER1 - Routing - controlled impedance pairs and general routing
Prepreg
GND - Power Plane
0.004" Prepreg
3.3V - Power Plane
Prepreg
INNER2 - Controlled Impedance and general routing
Prepreg
BOTTOM- Routing- Flood with copper where possible

Layout:
"Front" refers to the edge of the board to the right when looking at the component side of the board with PCI connector down.
Lay out LVDS pairs according to recommendations in Ch. 4 of http://www.national.com/appinfo/lvds/files/LOM_2.pdf.
Locate comparators and logic near front panel.
Locate DB-9 and LEMO connectors near each other.
Locate test connector at top (as close to top as reasonable),
Locate harmonica connector at back of board with openings facing up.
Space harmonica connector at least 1/2" down from top edge of board to allow for cable routing inside computer.
Locate LVDS drivers near harmonica connector.
MAKE LVDS PAIRS BETWEEN DRIVER AND HARMONICA CONNECTOR ALL THE SAME LENGTH!!!
Match lengths of + and - LVDS lines in pairs. (see reference)
Jumper footprints and open-ckt footprints should be the same size to permit easy configuration change.

Build:
Both Y1 and Y2 cannot be mounted at the same time.

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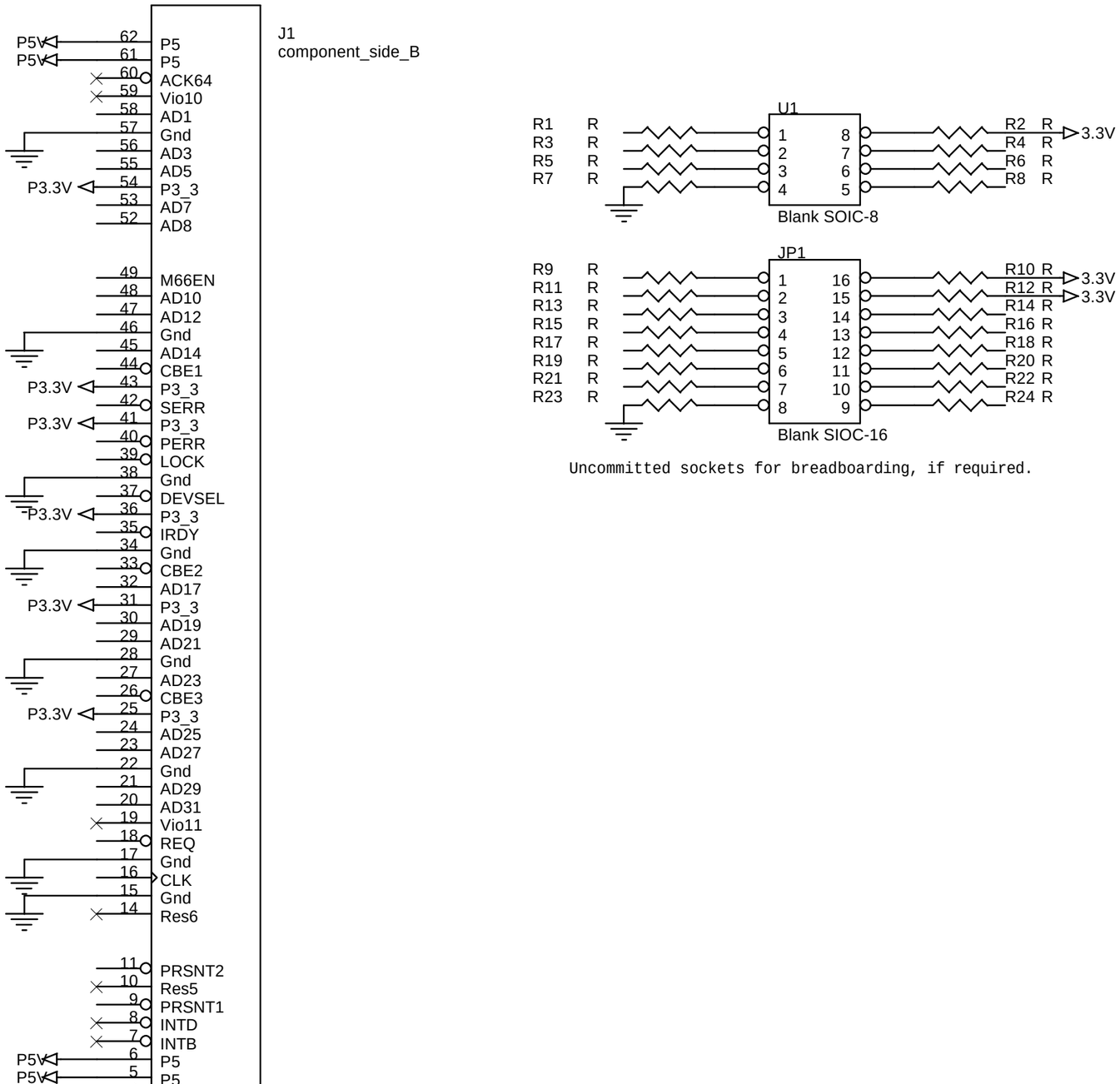
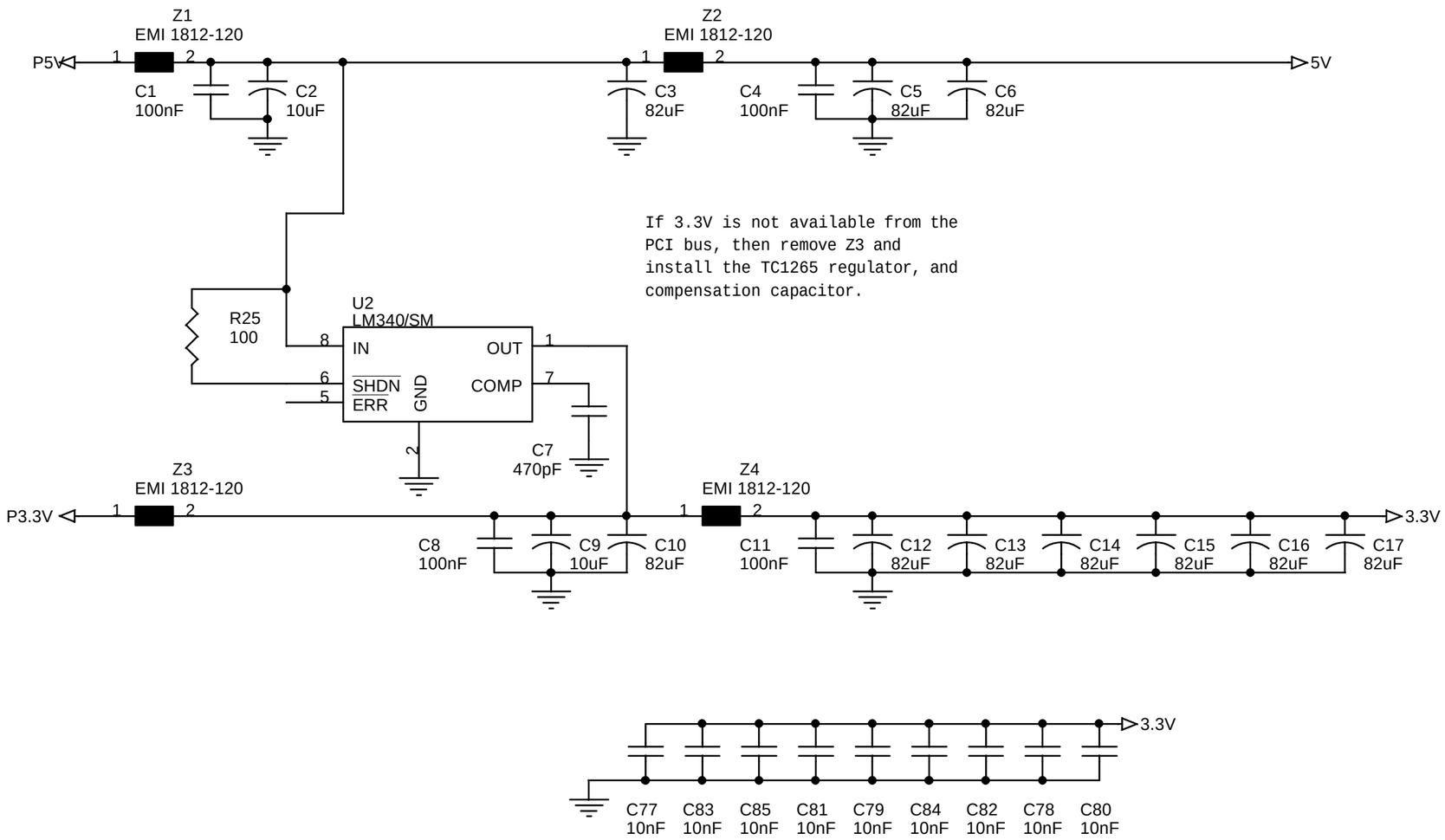
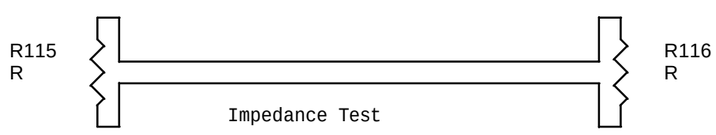
Title	Fabrication (Rev A, 2/26/04, As Built)	
Size A	Document Number DSB-Sheet1	Rev A
Date: Friday, April 09, 2004	Sheet 1 of 4	



Uncommitted sockets for breadboarding, if required.

Title	Mechanical (Rev A, 2/26/04, As Built)	
Size A	Document Number DSB-Sheet2	Rev A
Date: Friday, April 09, 2004	Sheet 2 of 4	





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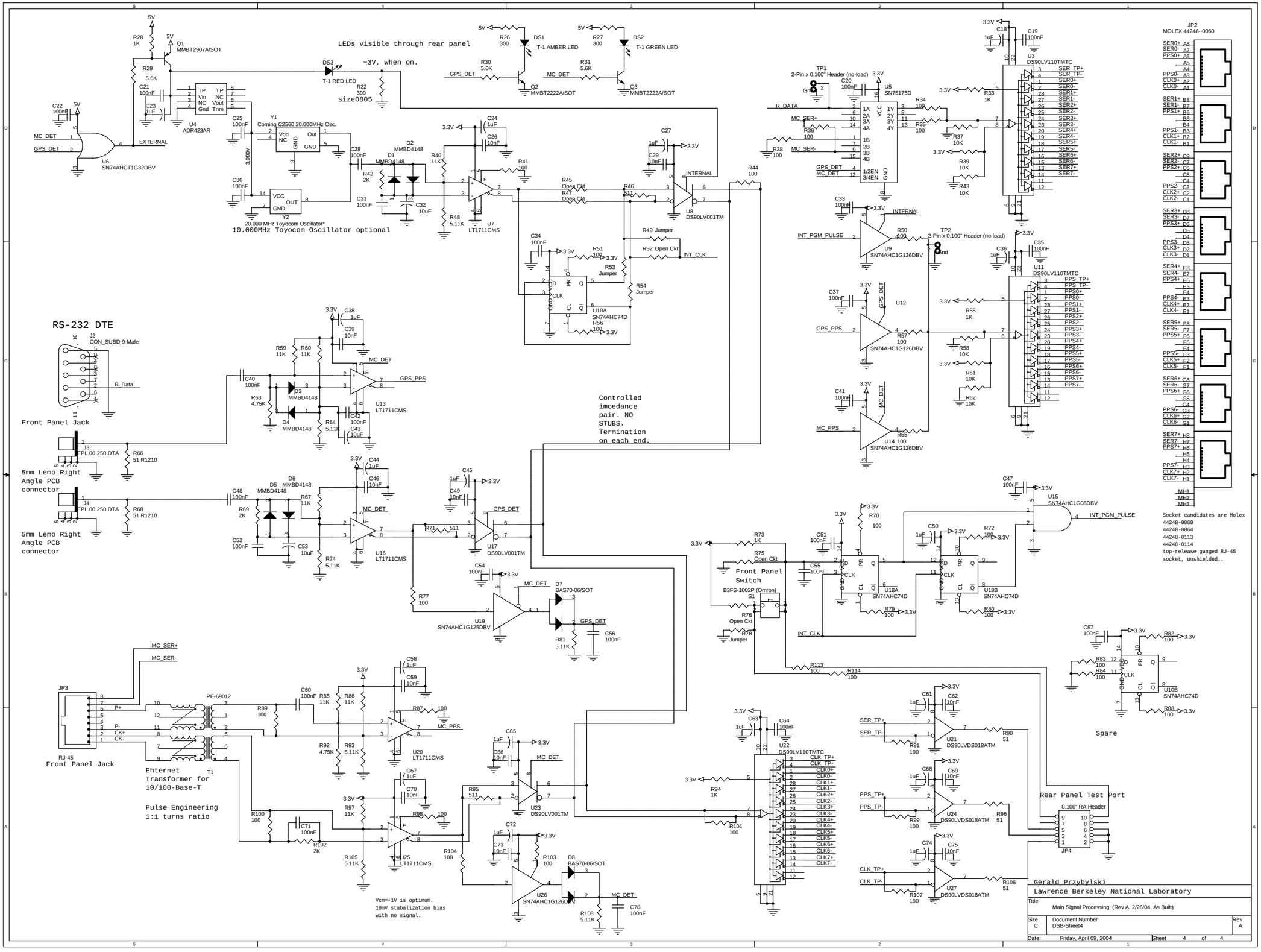
Title	Power (Rev A, 2/26/04, As Built)	
Size A	Document Number DSB-Sheet 3	Rev A
Date: Friday, April 09, 2004	Sheet 3 of 4	


LEDs visible through rear panel
~3V, when on.
T-1 RED LED
T-1 AMBER LED
T-1 GREEN LED
size0805
Q1 MMBT2907A/SOT
Q2 MMBT2222A/SOT
Q3 MMBT2222A/SOT
U4 ADR423AR
U6 SN74AHCT1G32DBV
Y1 Coming C2560 20.000MHz Osc.
Y2 20.000 MHz Toyocom Oscillator*
10.000MHz Toyocom Oscillator optional
U7 LT1711CMS
U8 DS90LV001TM
U10A SN74AHC74D
TP1 2-Pin x 0.100" Header (no-load)
U5 SN75175D
U3 DS90LV110TMTC
TP2 2-Pin x 0.100" Header (no-load)
U9 SN74AHC1G126DBV
U11 DS90LV110TMTC
U12 SN74AHC1G126DBV
U14 SN74AHC1G126DBV
JP2 MOLEX 44248--0060
Socket candidates are Molex
44248-0060
44248-0064
44248-0113
44248-0114
top-release ganged RJ-45
socket, unshielded..
RS-232 DTE
J2 CON_SUBD-9-Male
Front Panel Jack
J3 EPL.00.250.DTA
5mm Lemo Right Angle PCB connector
J4 EPL.00.250.DTA
5mm Lemo Right Angle PCB connector
U13 LT1711CMS
U16 LT1711CMS
U17 DS90LV001TM
U19 SN74AHC1G125DBV
Controlled imoedance pair. NO STUBS. Termination on each end.
U15 SN74AHC1G08DBV
Front Panel Switch
B3FS-1002P (Omron)
U18A SN74AHC74D
U18B SN74AHC74D
JP3
RJ-45 Front Panel Jack
PE-69012
Ehternet Transformer for 10/100-Base-T
T1
Pulse Engineering 1:1 turns ratio
U20 LT1711CMS
U23 DS90LV001TM
U25 LT1711CMS
U26 SN74AHC1G126DBV
Vcm=+1V is optimum.
10mV stabalization bias
with no signal.
U22 DS90LV110TMTC
U21 DS90LVDS018ATM
U24 DS90LVDS018ATM
U27 DS90LVDS018ATM
U10B SN74AHC74D
Spare
Rear Panel Test Port
0.100" RA Header
JP4
Gerald Przybylski
Lawrence Berkeley National Laboratory
Title
Main Signal Processing (Rev A, 2/26/04, As Built)
Size C
Document Number DSB-Sheet4
Rev A
Date: Friday, April 09, 2004
Sheet 4 of 4