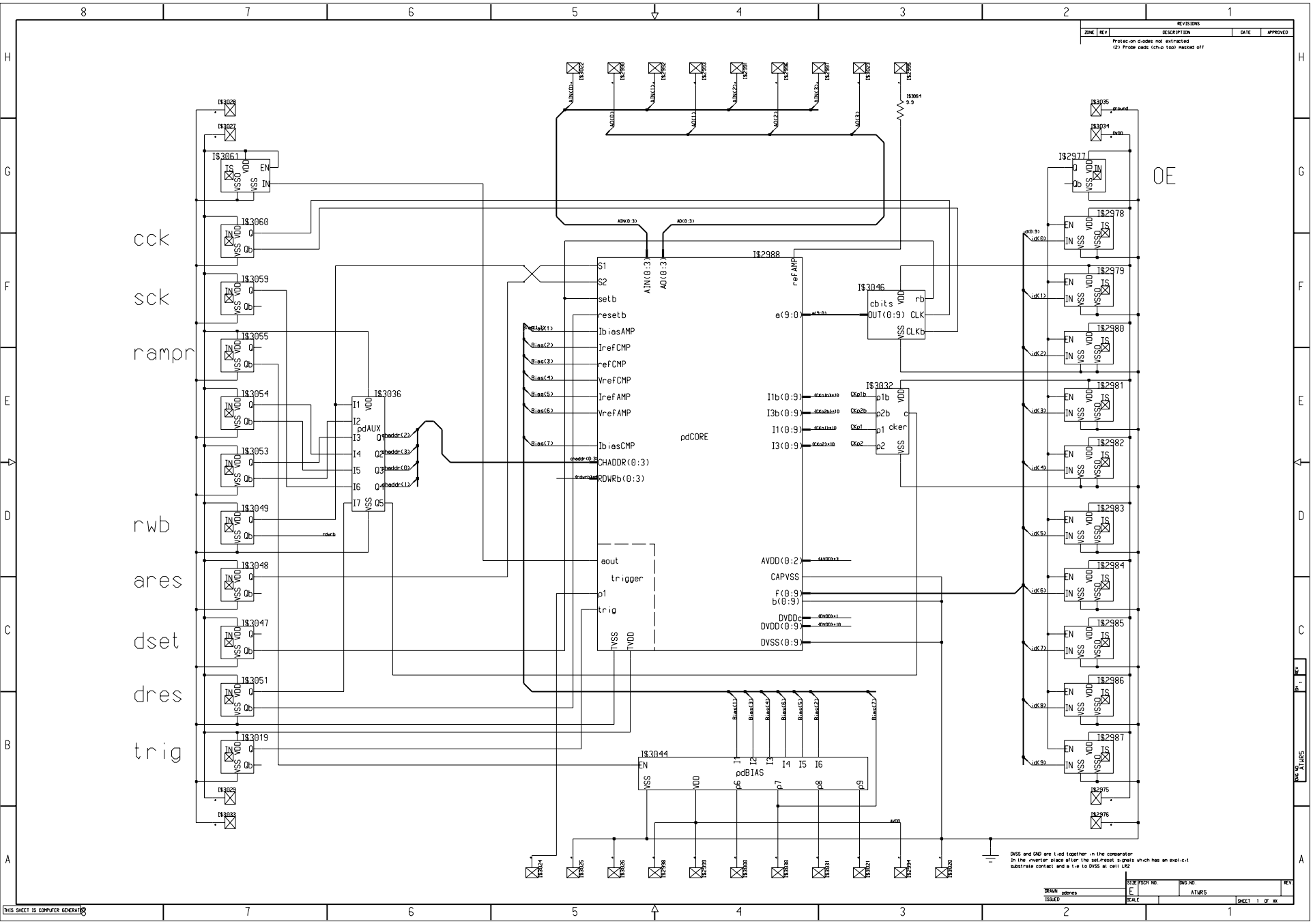
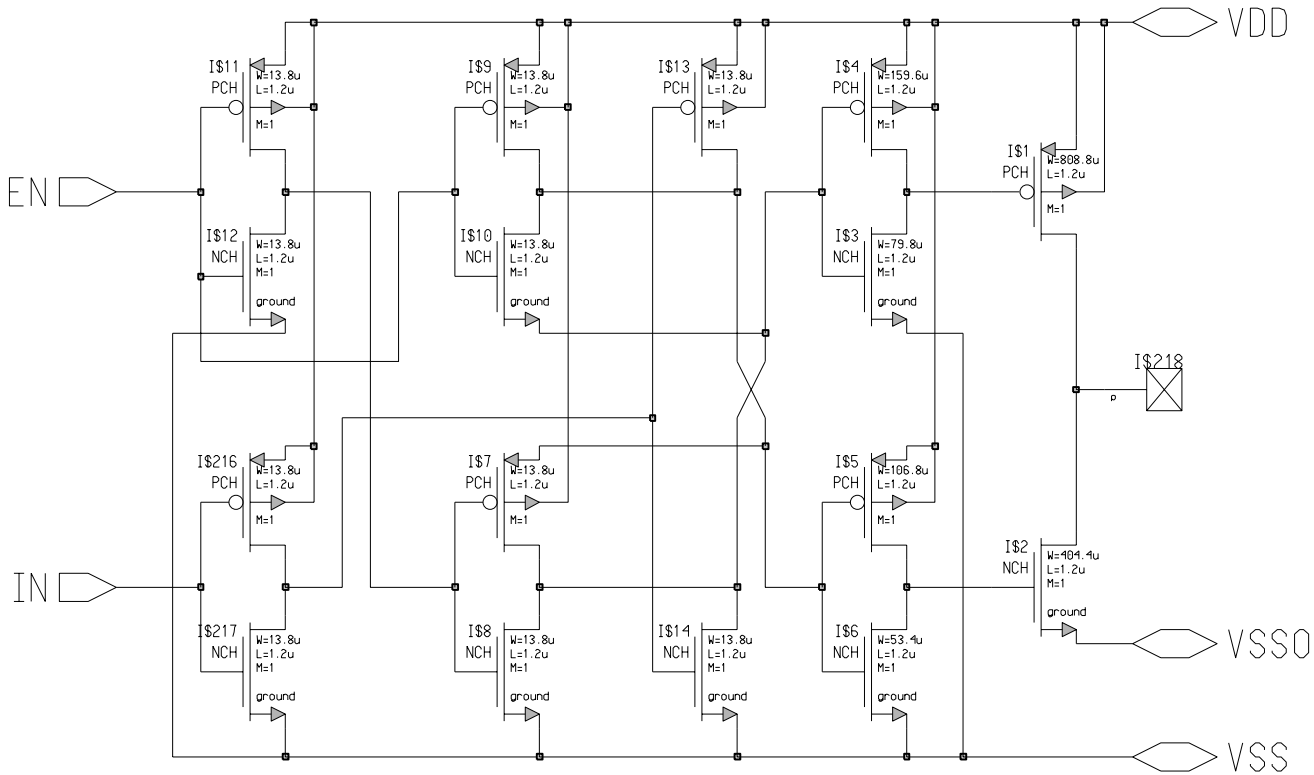


Design Pathname	Version	Edited By	Last Edit
/home/engFile2/did/pdenes/IceCube/ATWD/menATWR/sch/ATWR5 schematic sheet1	1	pdenes	Saturday, february 23, 2002, 4:10:37 pm

DWG.NO zpadts | SH 1 | REV.

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED
		LVS OK 23 Feb 02		



DRAWN pdenes	SIZE B	FSCM NO.	DWG.NO. zpadts	REV.
ISSUED	SCALE		SHEET 1 OF XX	

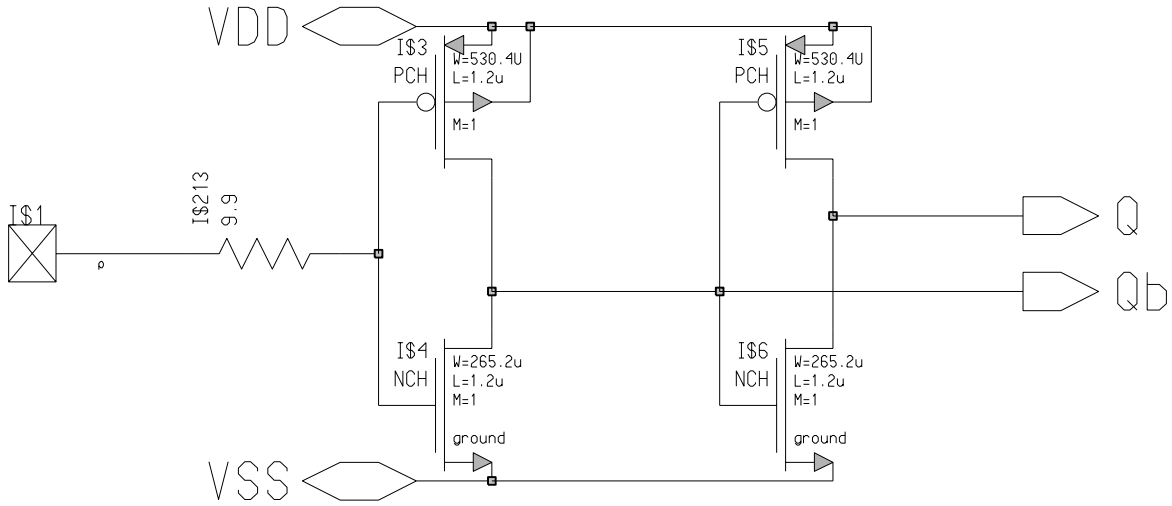
THIS SHEET IS COMPUTER GENERATED

Design Pathname	Version	Edited By	Last Edit
/home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch/zpadts schematic sheet1	1	pdenes	Friday, January 25, 2002, 10:39:10 am

DWG.NO zpadin3	SH 1	REV.

REVISIONS

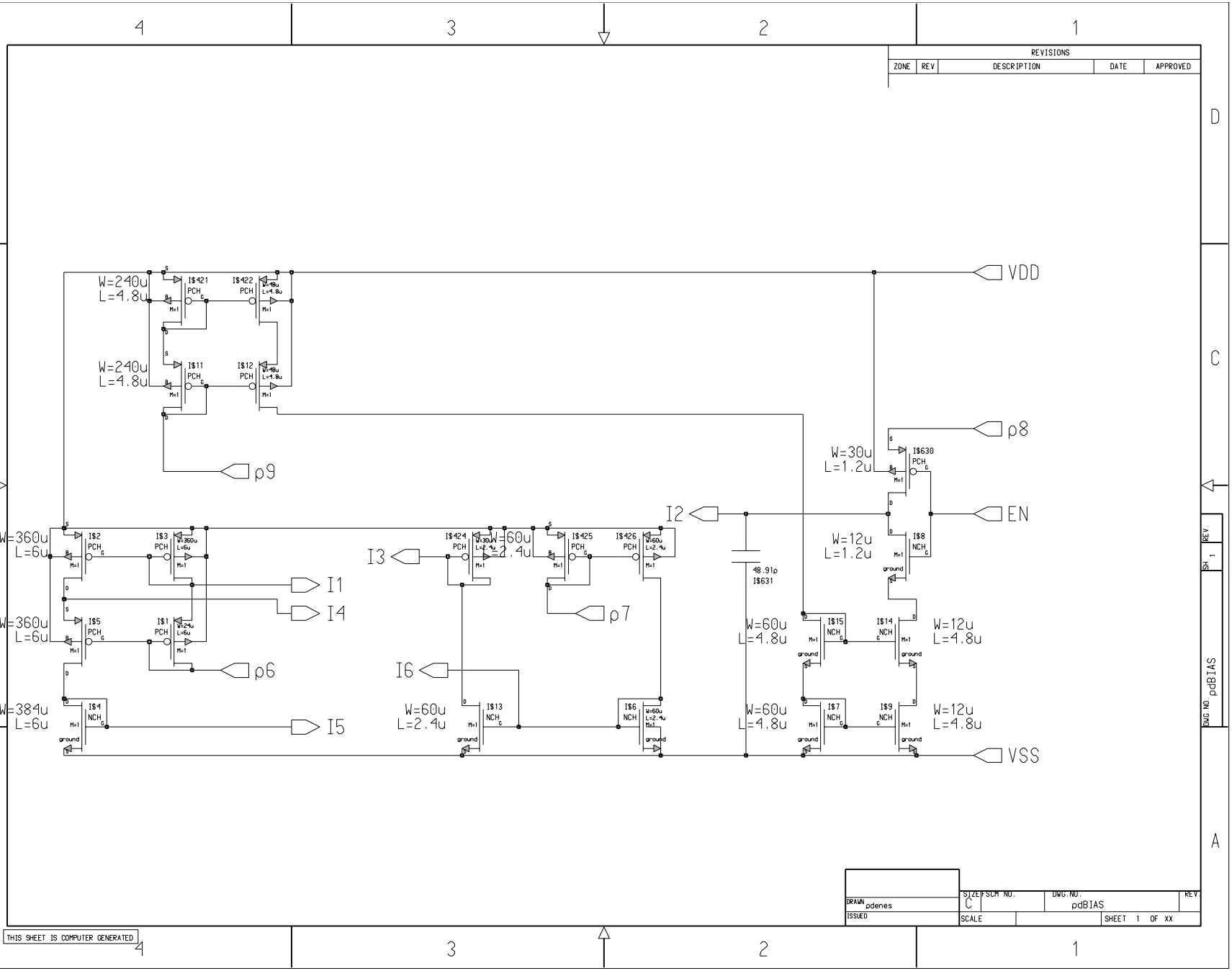
REV	DESCRIPTION	DATE	APPROVED
	LVS OK 25JAN02		



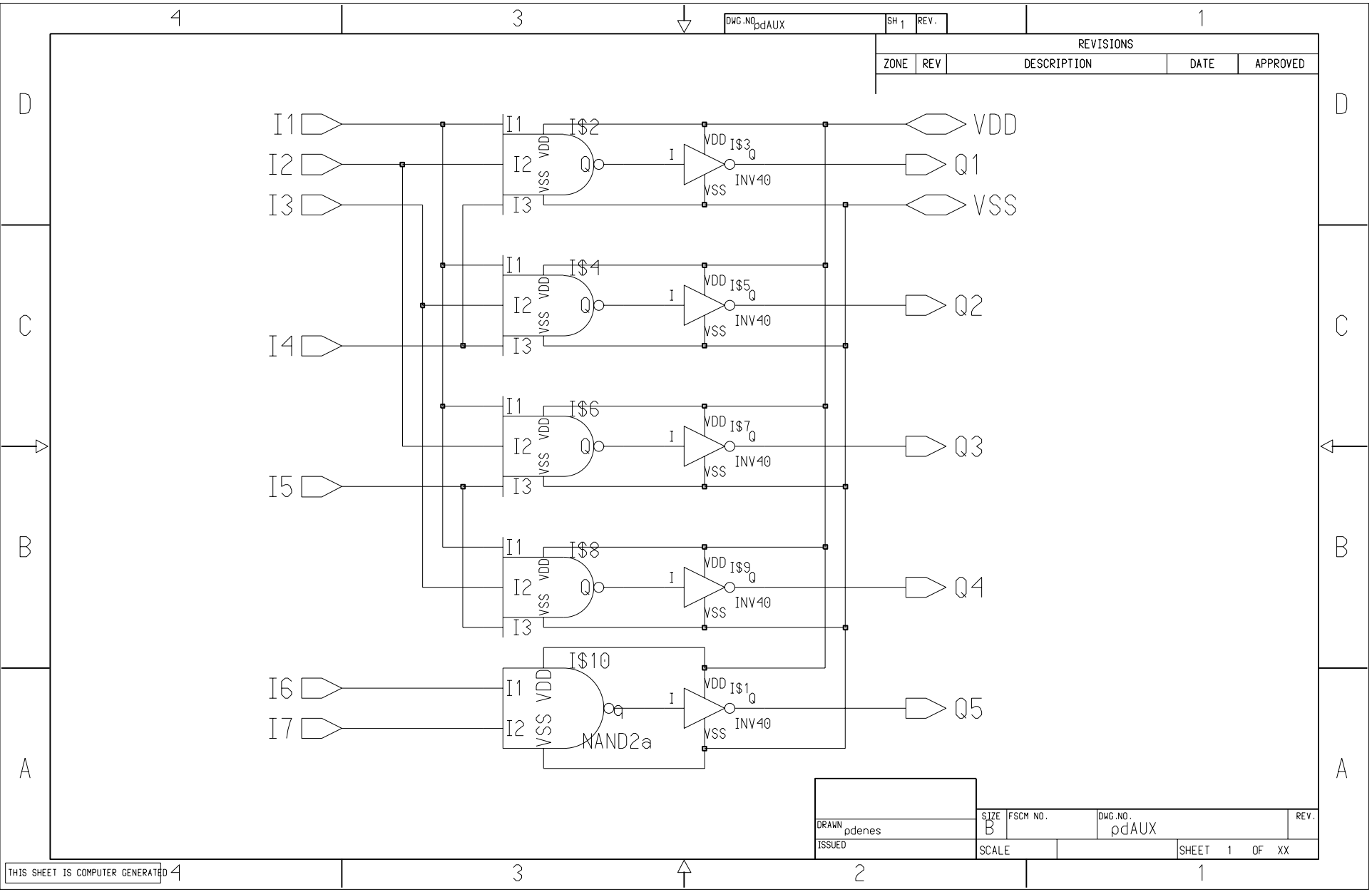
DRAWN pdenes	SIZE A	FSCM NO.	DWG.NO. zpadin3	REV.
ISSUED	SCALE		SHEET 1 OF XX

THIS SHEET IS COMPUTER GENERATED

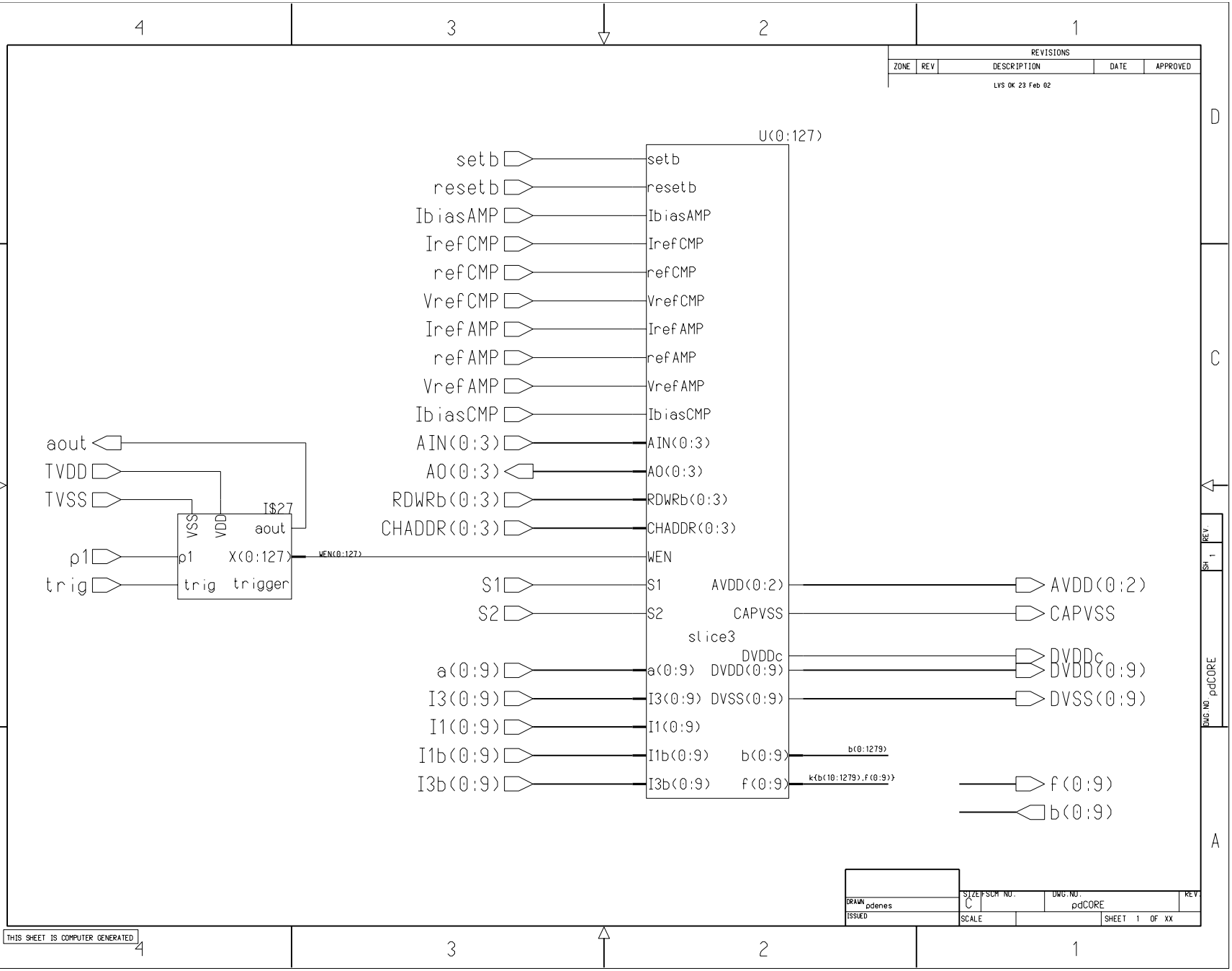
Design Pathname:	Version:	Edited By:	Last Edit:
/home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch/zpadin3 schematic sheet1	1	pdenes	Friday, January 25, 2002, 8:59:22 am



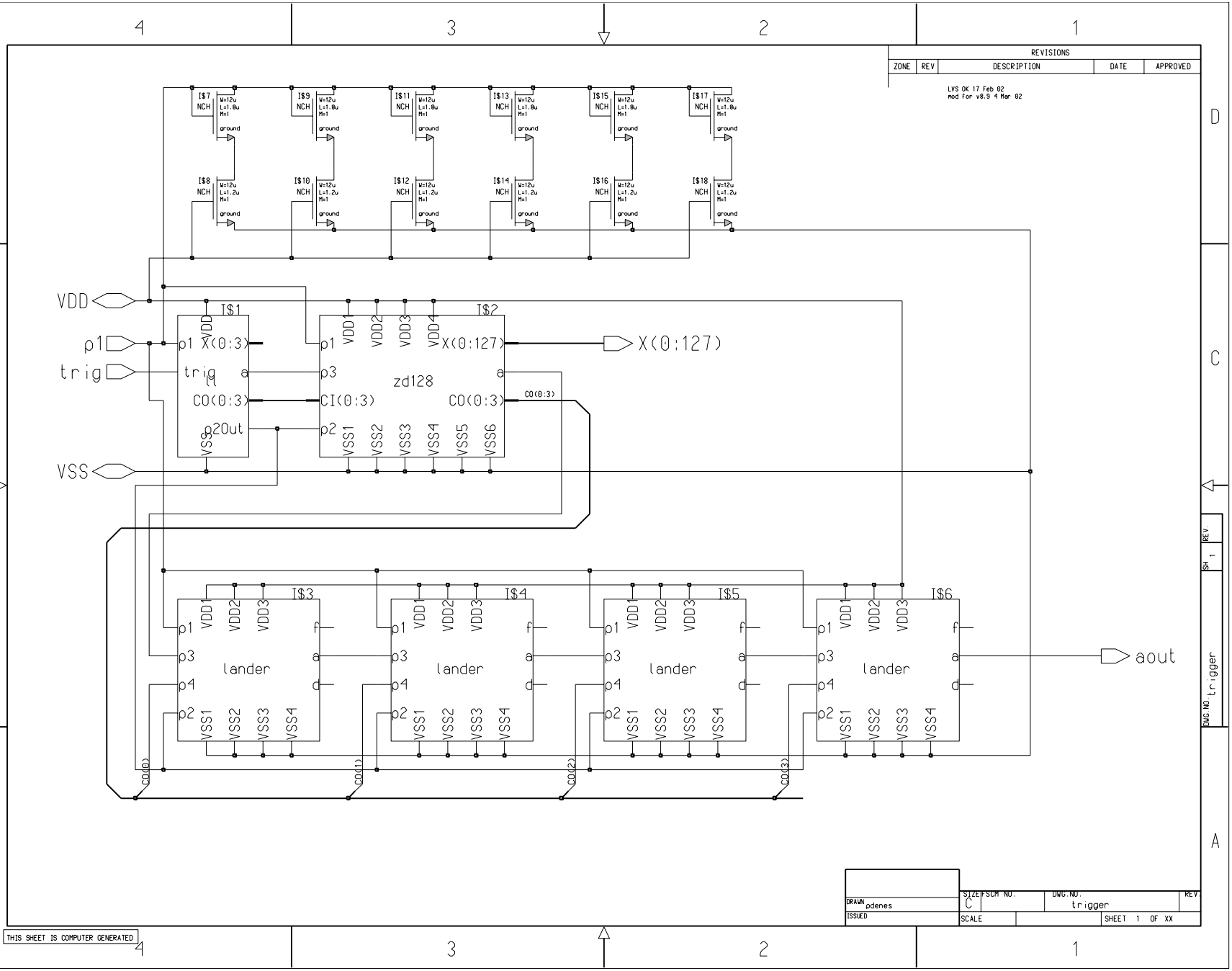
Design Pathname	Version	Edited By	Last Edit
/home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch/pdBIAS schematic sheet1	1	pdenes	Saturday, February 23, 2002, 6:54:47 pm



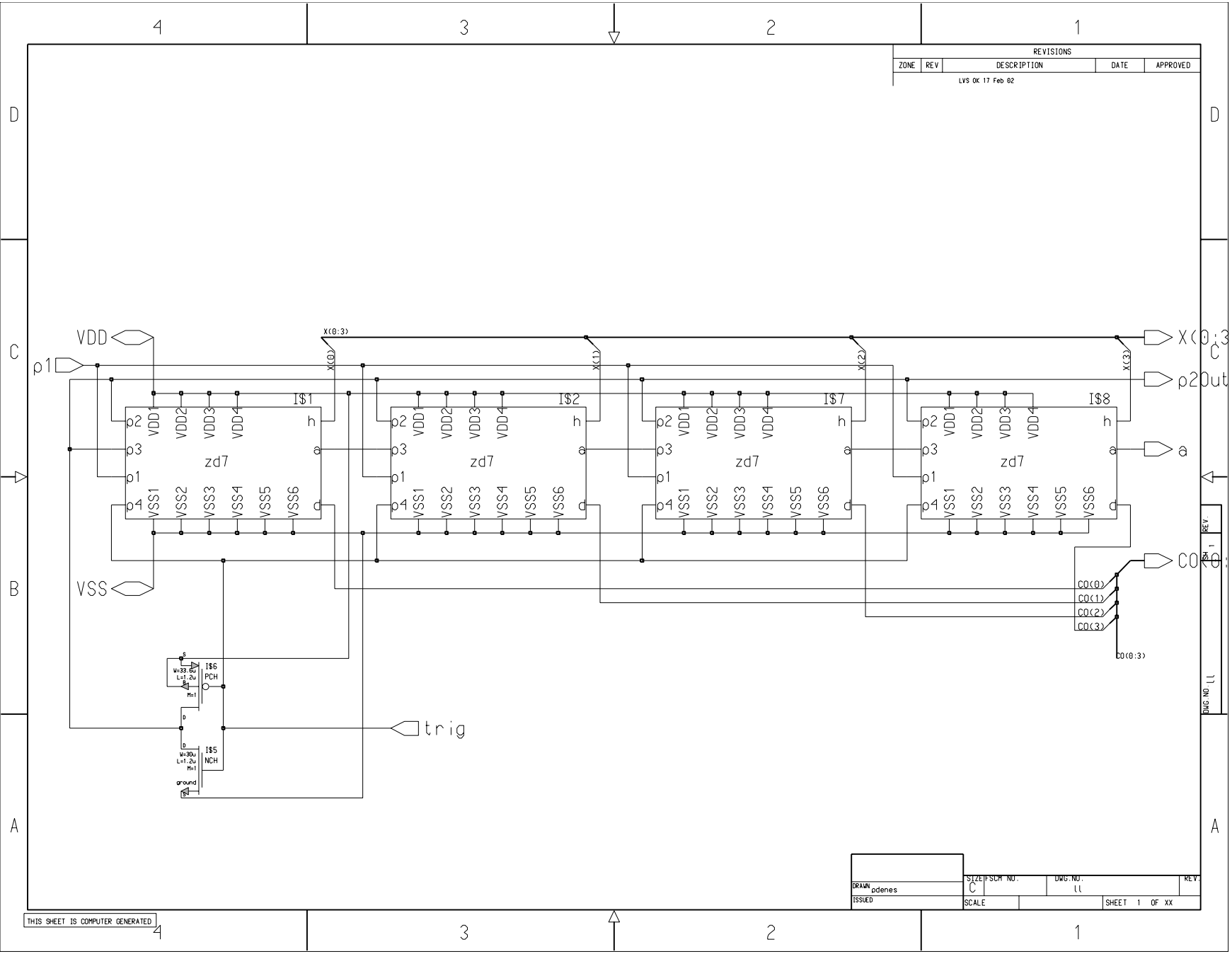
Design Pathname	Version	Edited By	Last Edit
/home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch/pdAUX schematic sheet1	1	pdenes	Saturday, February 23, 2002, 9:08:13 pm



Design Pathname	Version	Edited By	Last Edit
/home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch/pdCORE schematic sheet1	1	pdenes	Friday, February 22, 2002, 6:32:44 pm

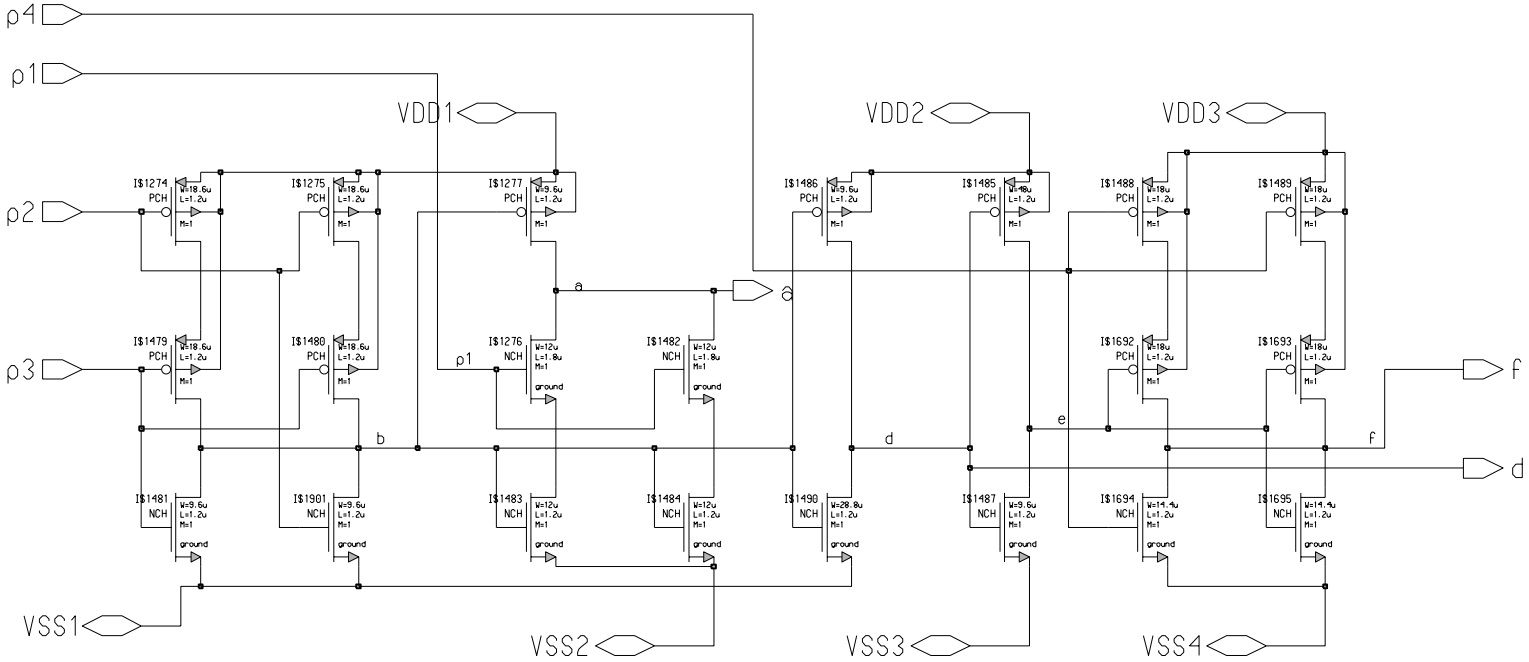


Design Pathname	Version	Edited By	Last Edit
/home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch/trigger schematic sheet1	1	pdenes	Sunday, February 17, 2002, 1:03:14 pm



Design Pathname	Version	Edited By	Last Edit
/home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch/ll schematic sheet1	1	pdenes	Sunday, February 17, 2002, 11:55:13 am

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
		LVS OK 17 Feb 02		

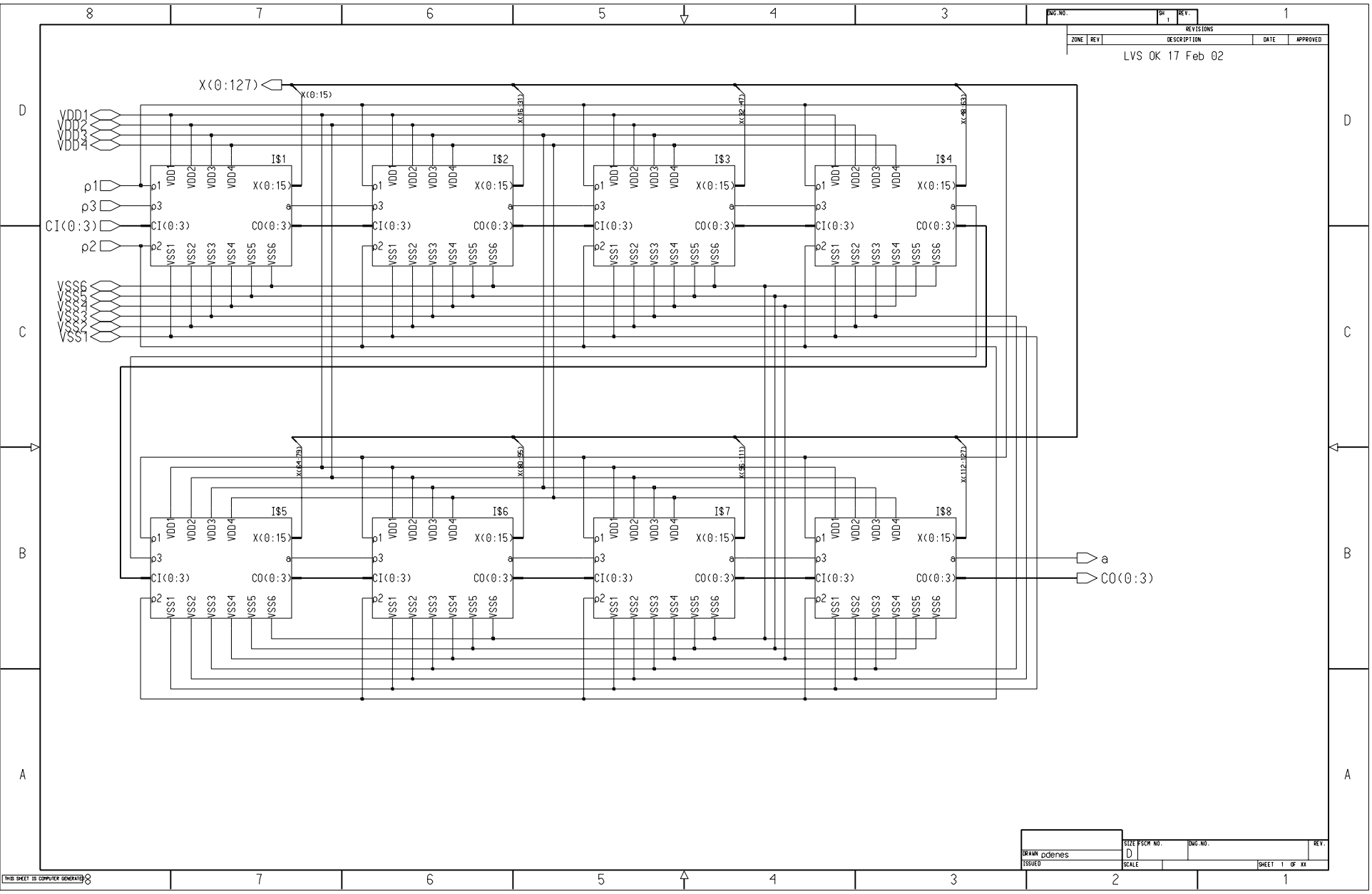


DRAWN pdenes	SIZE C	SCH NO.	DWG.NO. lander	REV
ISSUED	SCALE		SHEET 1 OF XX

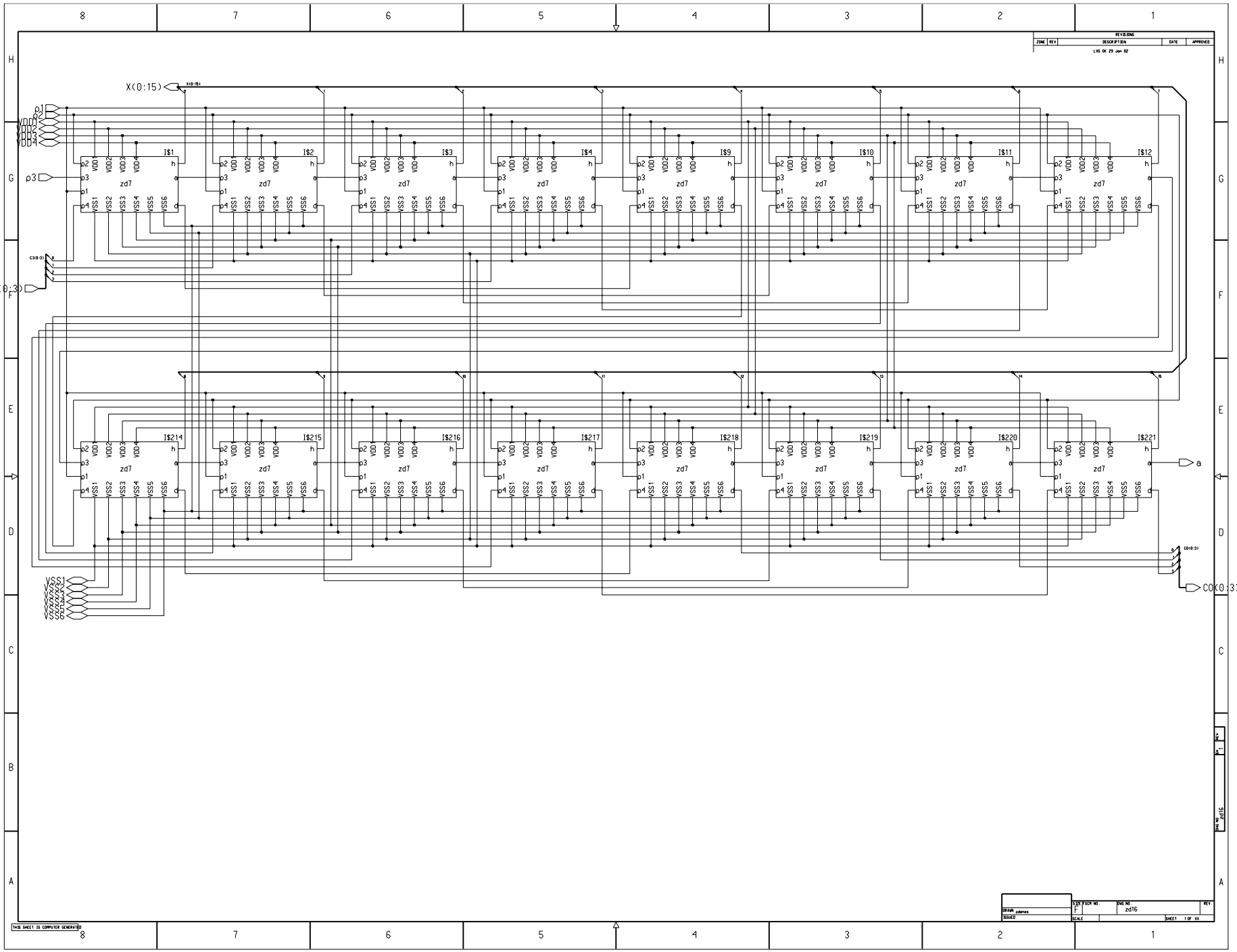
REV SH 1 DWG.NO. lander

THIS SHEET IS COMPUTER GENERATED

Design Pathname	Version	Edited By	Last Edit
/home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch/lander schematic sheet1	23	pdenes	Sunday, February 17, 2002, 12:29:47 pm



Design Pathname	Version	Edited By	Last Edit
/home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch/zd128 schematic sheet1	1	pdenes	Thursday, January 31, 2002, 9:47:02 am

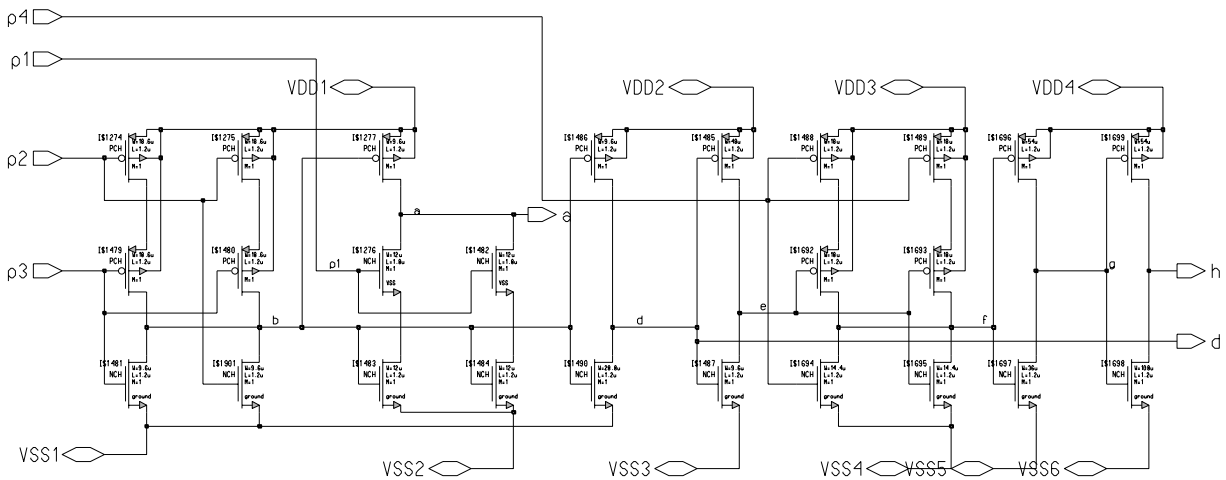


Design Pathname	Version	Edited By	Last Edit
/home/engfile2/did/pdenes/IceCube/ATWD/nenATWR/sch/zd16 schematic sheet1	1	pdenes	Tuesday, January 29, 2002, 10:37:43 am

DWG.NO.	SH 1	REV.

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED
		LVS OK 20.01.02 PD mod for v8.9 3 Mar 02		



DRAWN pdenes	SIZE D	FSCM NO.	DWG.NO.	REV.
ISSUED	SCALE		SHEET 1 OF XX	

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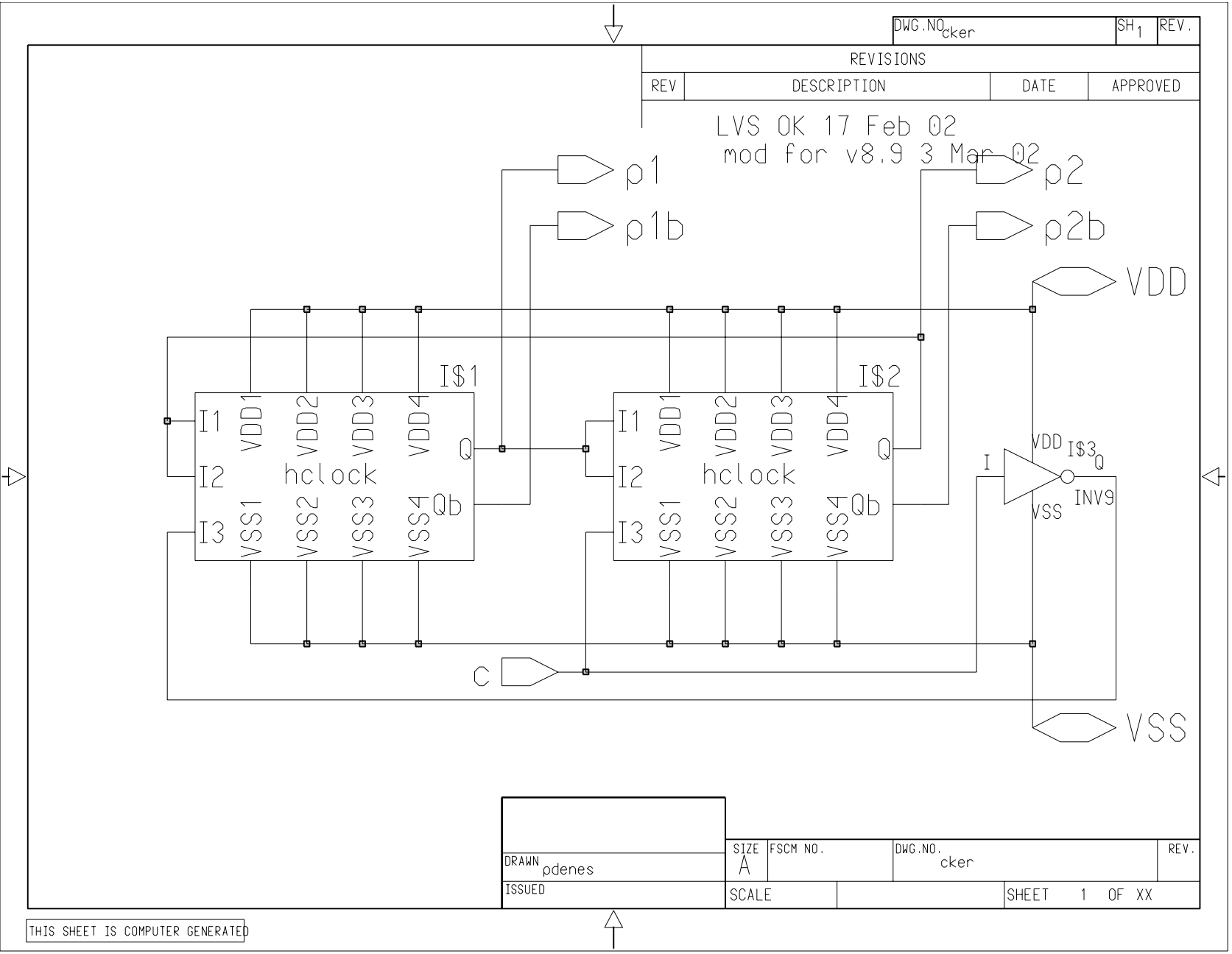
Design Pathname	Version	Edited By	Last Edit
/home/engfile2/did/pdenes/IceCube/ATWD/menATWR/zd7 schematic sheet1	1	pdenes	Saturday, January 19, 2002, 6:35:51 pm



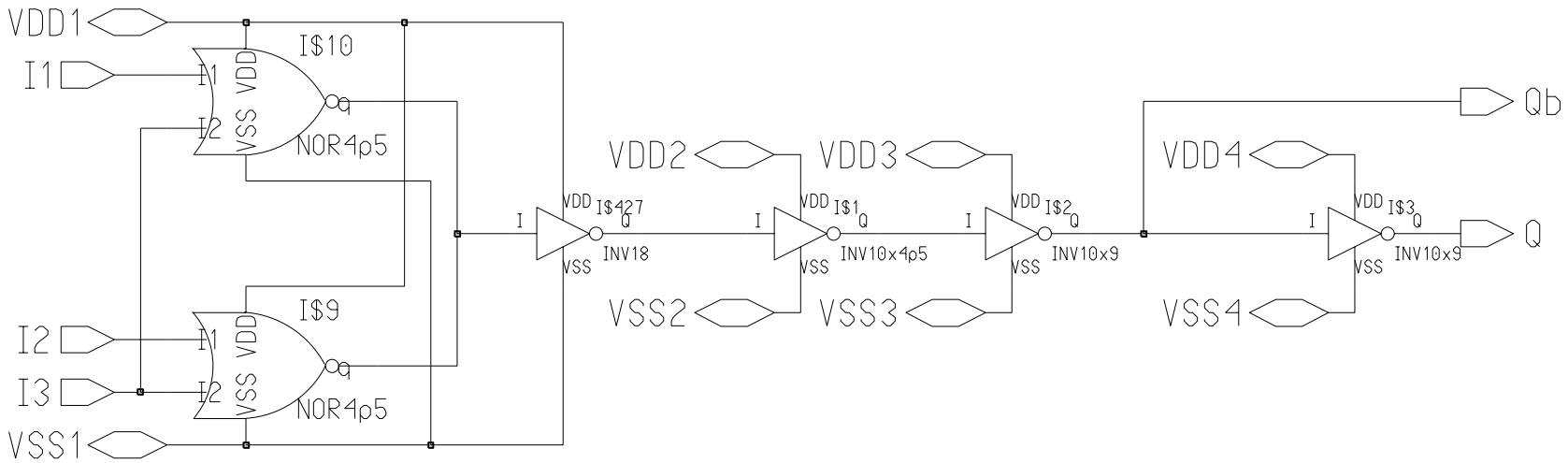
Design Pathname:	Version:	Edited By:	Last Edit:
/home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch/cker schematic sheet1	1	pdenes	Saturday, February 16, 2002, 9:48:59 pm

DWG.NO nor4p5 | SH 1 | REV.

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

LVS OK 16 Feb 02
mod for v8.9 3 Mar 02



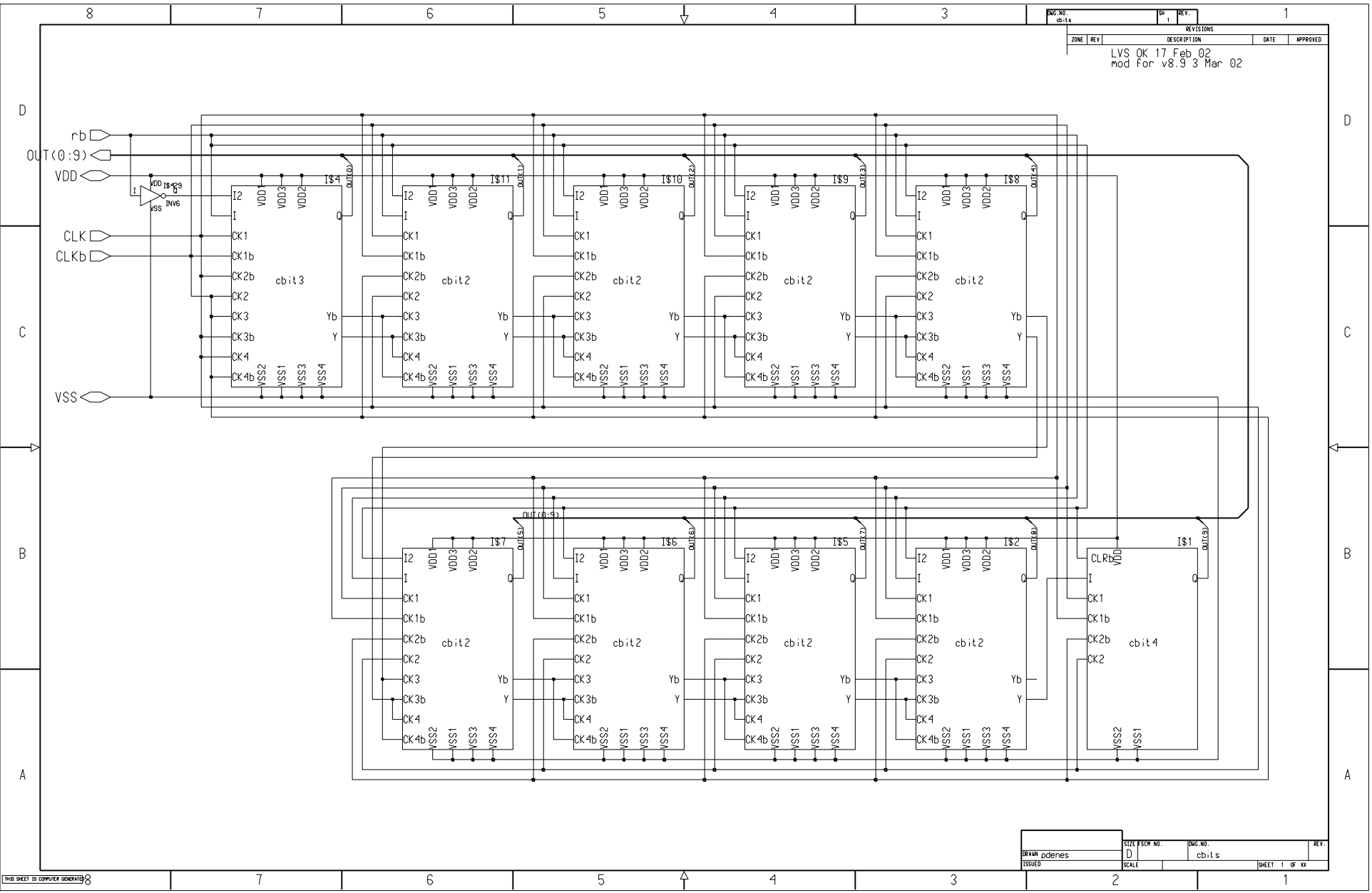
DRAWN pdenes
ISSUED

SIZE B | FSCM NO. | DWG.NO. nor4p5 | REV.

SCALE | SHEET 1 OF XX

THIS SHEET IS COMPUTER GENERATED

Design Pathname	Version	Edited By	Last Edit
/home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch/hclock schematic sheet1	1	pdenes	Saturday, February 16, 2002, 9:09:08 pm



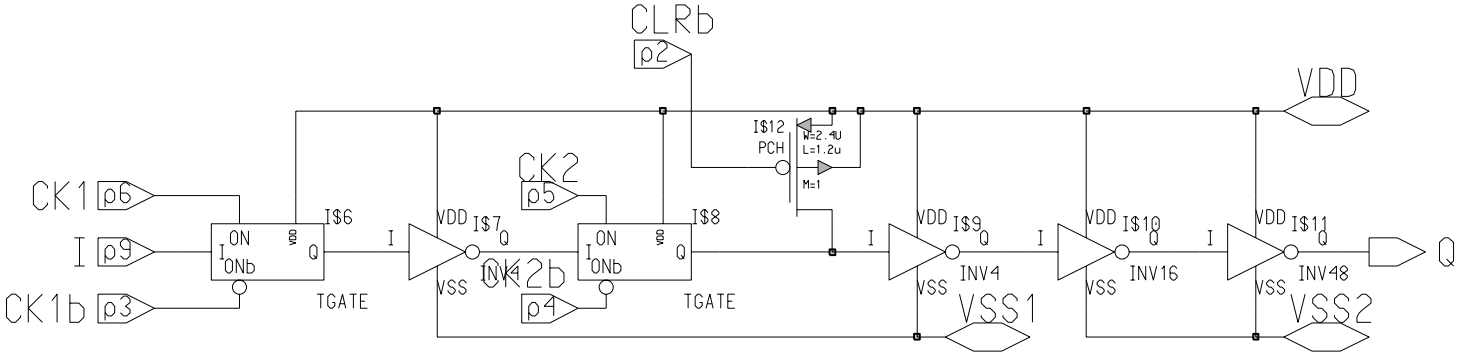
Design Pathname	Version	Edited By	Last Edit
/home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch/cbits schematic sheet1	1	pdenes	Sunday, February 17, 2002, 1:59:25 pm

DWG.NO cbit4 | SH 1 | REV.

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

LVS OK 24JAN02
mod for v8.9 3 Mar 02

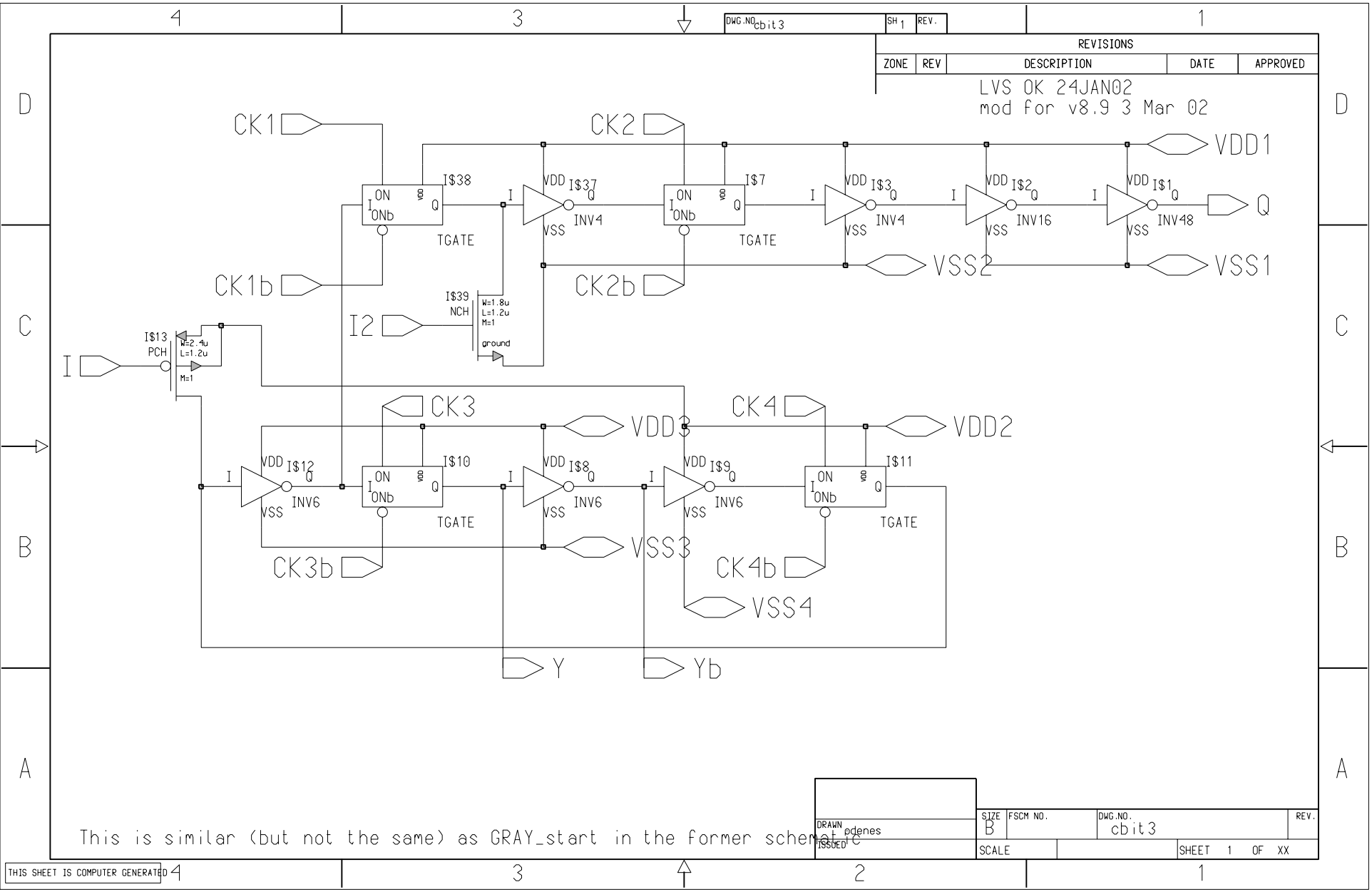


This appears to correspond to GRAY_end in the former schematics

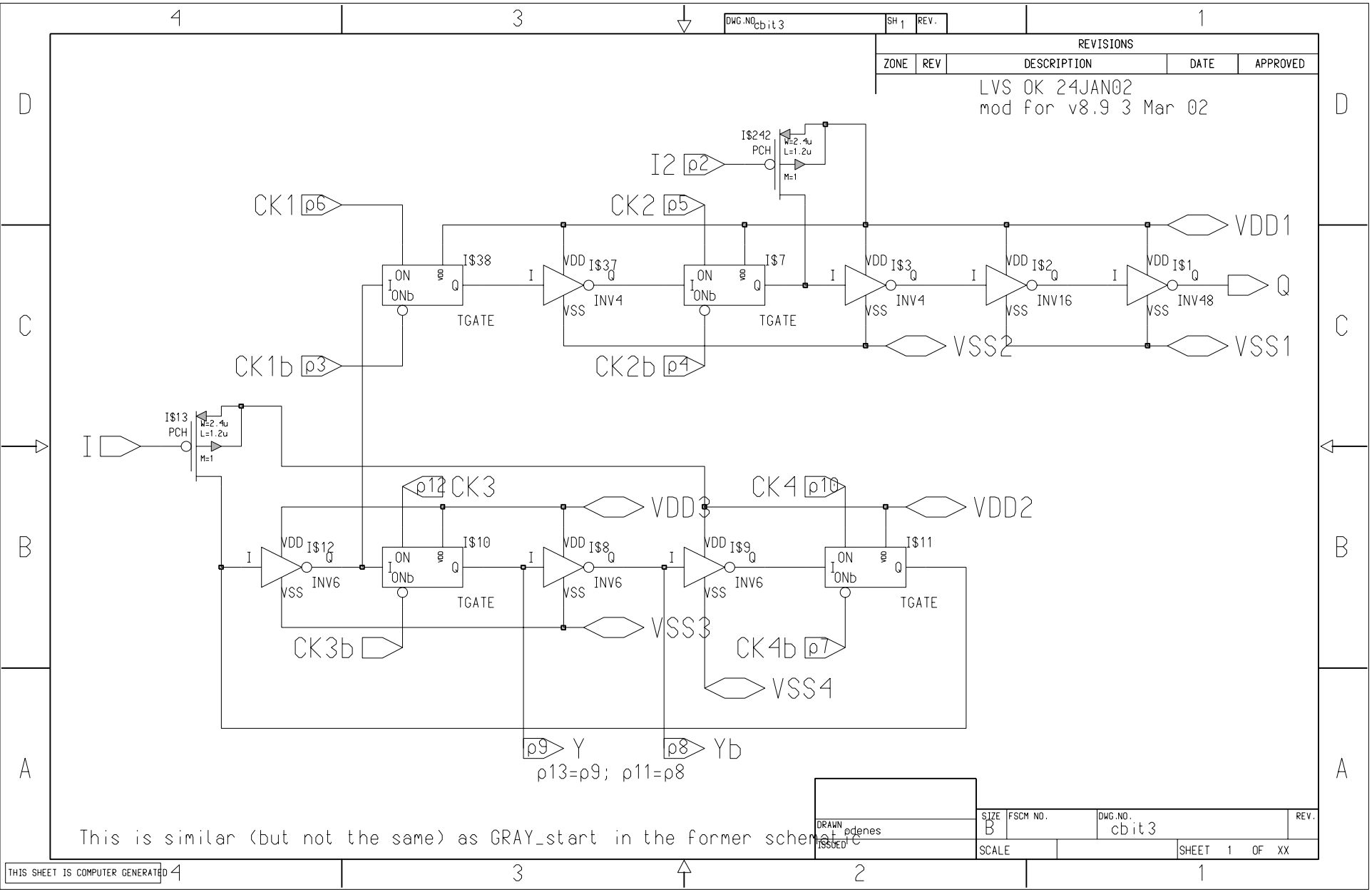
DRAWN pdenes	SIZE B	FSCM NO.	DWG.NO. cbit4	REV.
ISSUED	SCALE		SHEET 1 OF XX	

THIS SHEET IS COMPUTER GENERATED

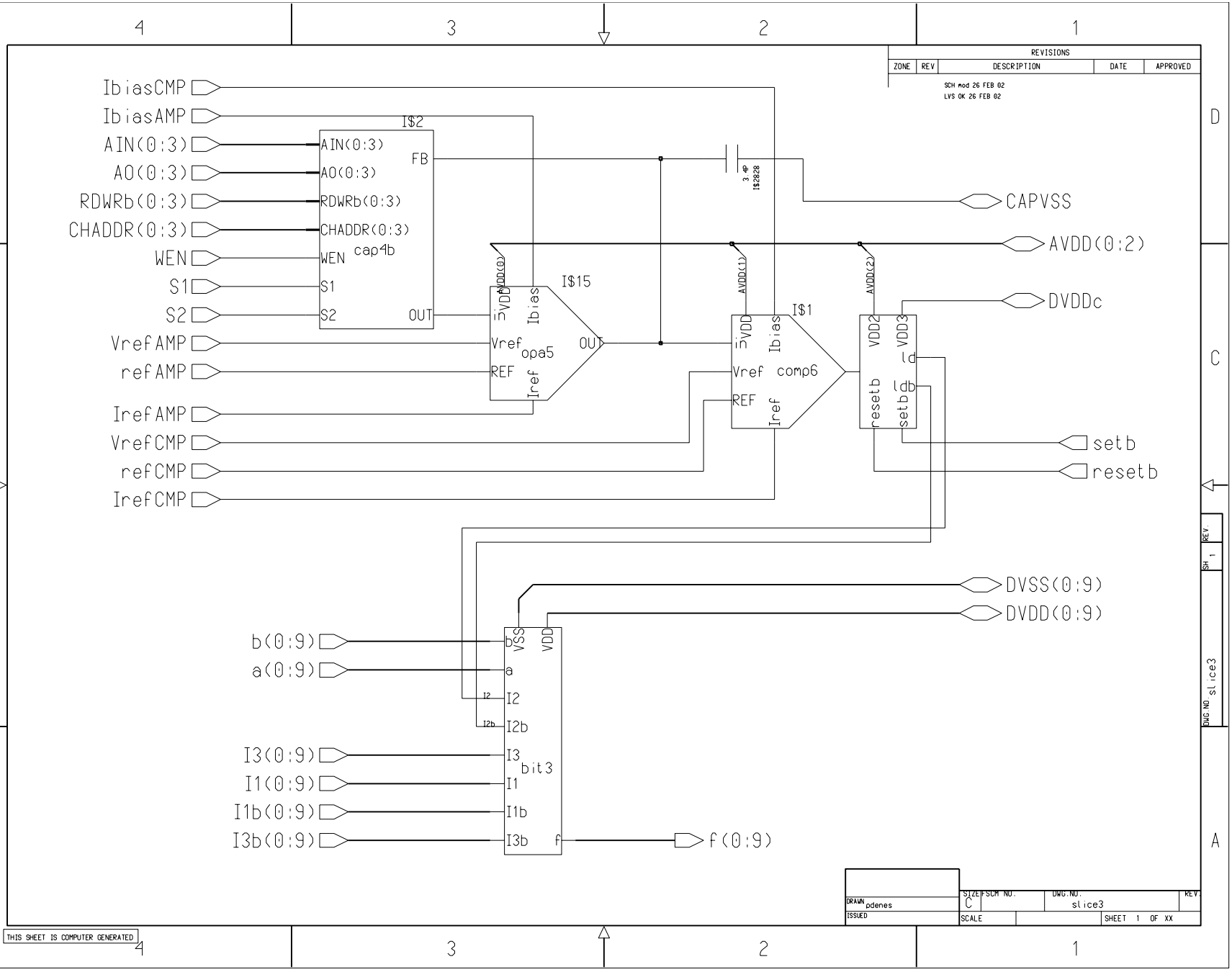
Design Pathname	Version	Edited By	Last Edit
/home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch/cbit4 schematic sheet1	1	pdenes	Thursday, January 24, 2002, 3:07:29 pm



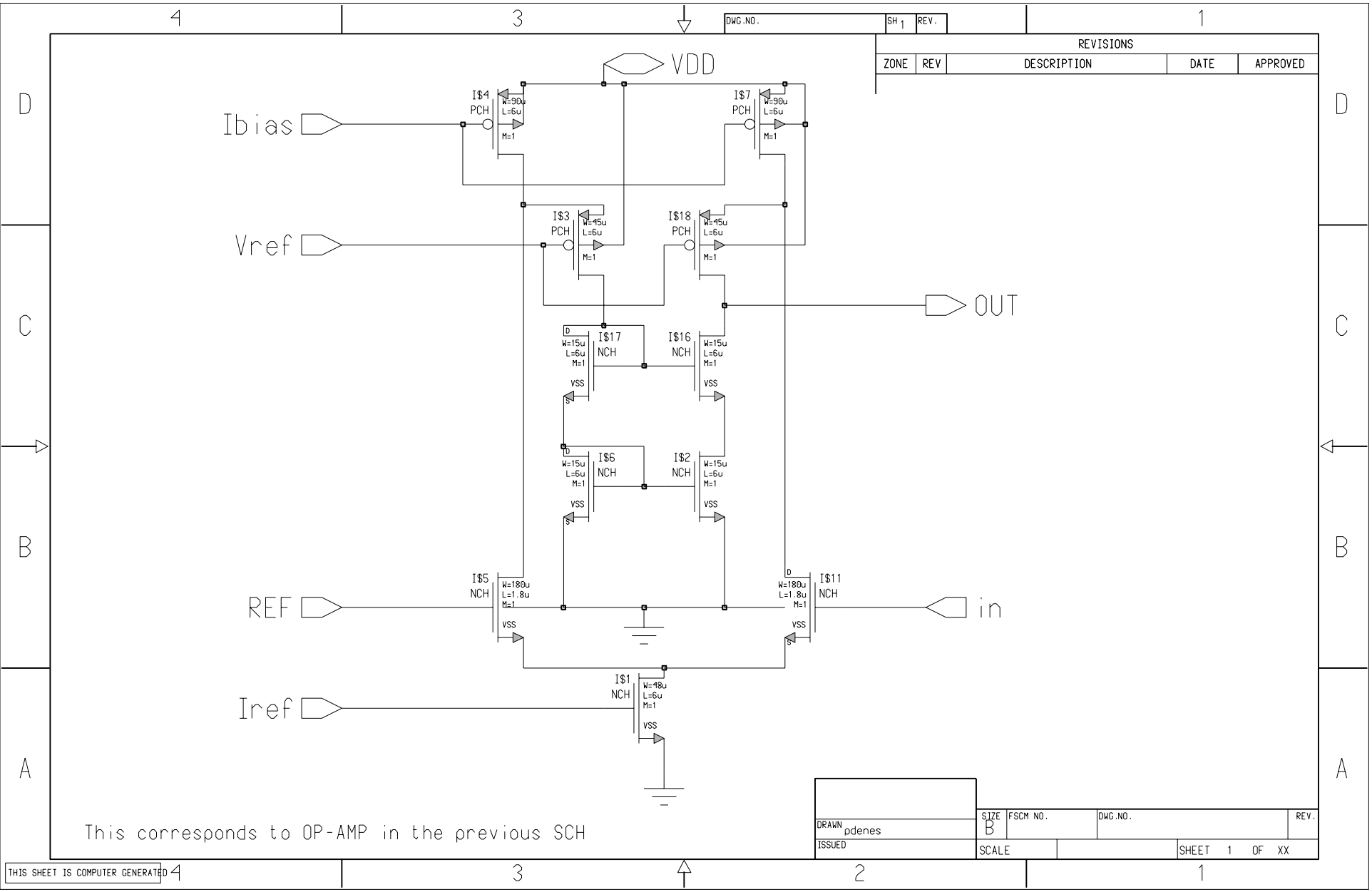
Design Pathname	Version	Edited By	Last Edit
/home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch/cbit3 schematic sheet1	1	pdenes	Thursday, January 24, 2002, 4:22:33 pm



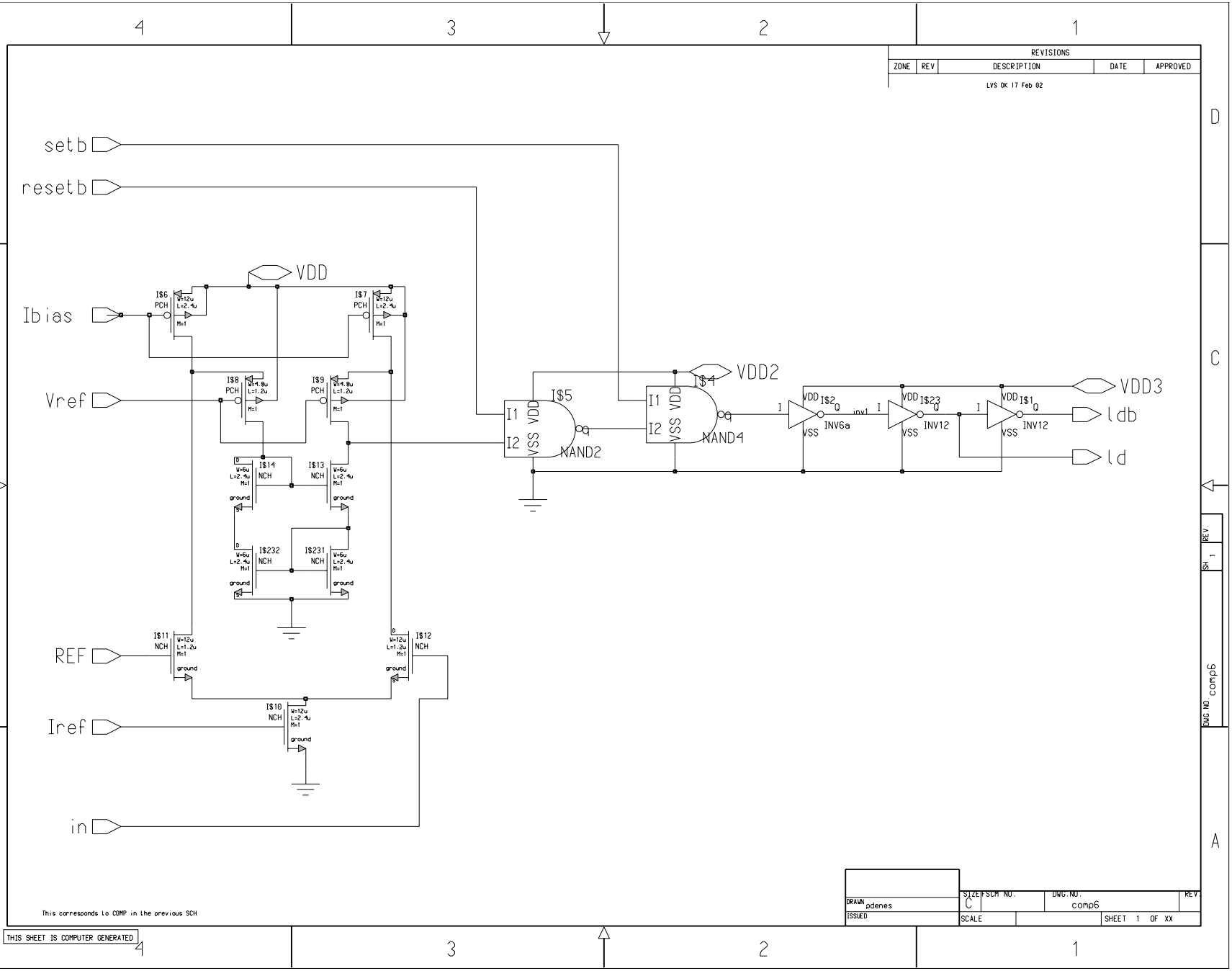
Design Pathname	Version	Edited By	Last Edit
/home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch/cbit2 schematic sheet1	9	pdenes	Friday, March 1, 2002, 10:30:27 am



Design Pathname	Version	Edited By	Last Edit
/home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch/slice3 schematic sheet1	15	pdenes	Friday, February 22, 2002, 4:46:48 pm



Design Pathname	Version	Edited By	Last Edit
/home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch/opa5 schematic sheet1	2	pdenes	Sunday, February 17, 2002, 9:50:12 am

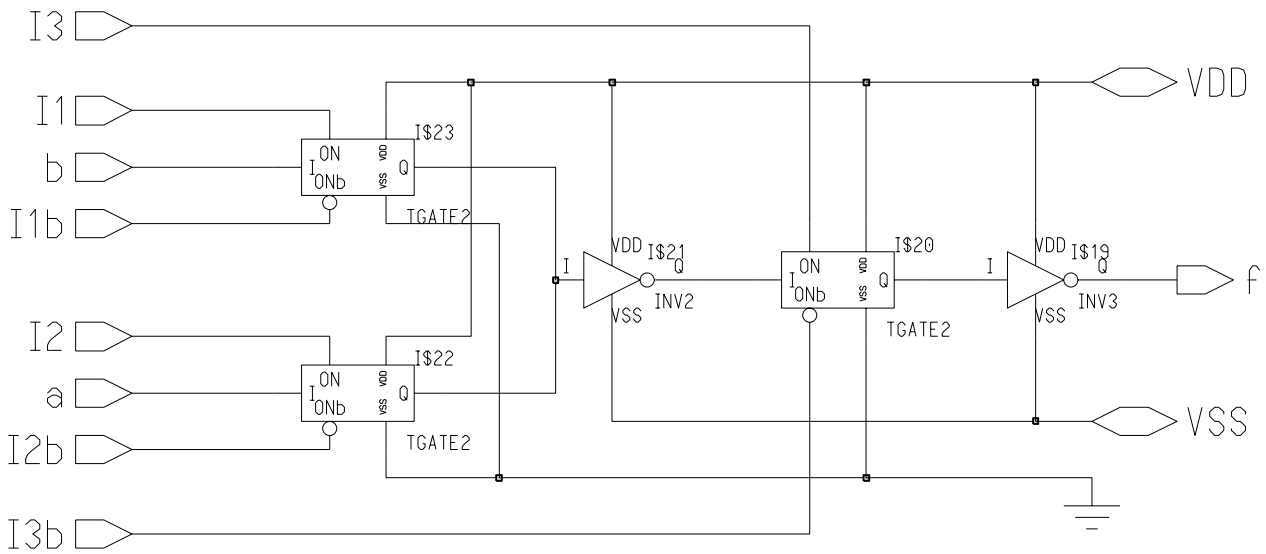


Design Pathname	Version	Edited By	Last Edit
/home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch/comp6 schematic sheet1	1	pdenes	Sunday, February 17, 2002, 10:31:31 am

DWG.NO bit3 | SH 1 | REV.

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED

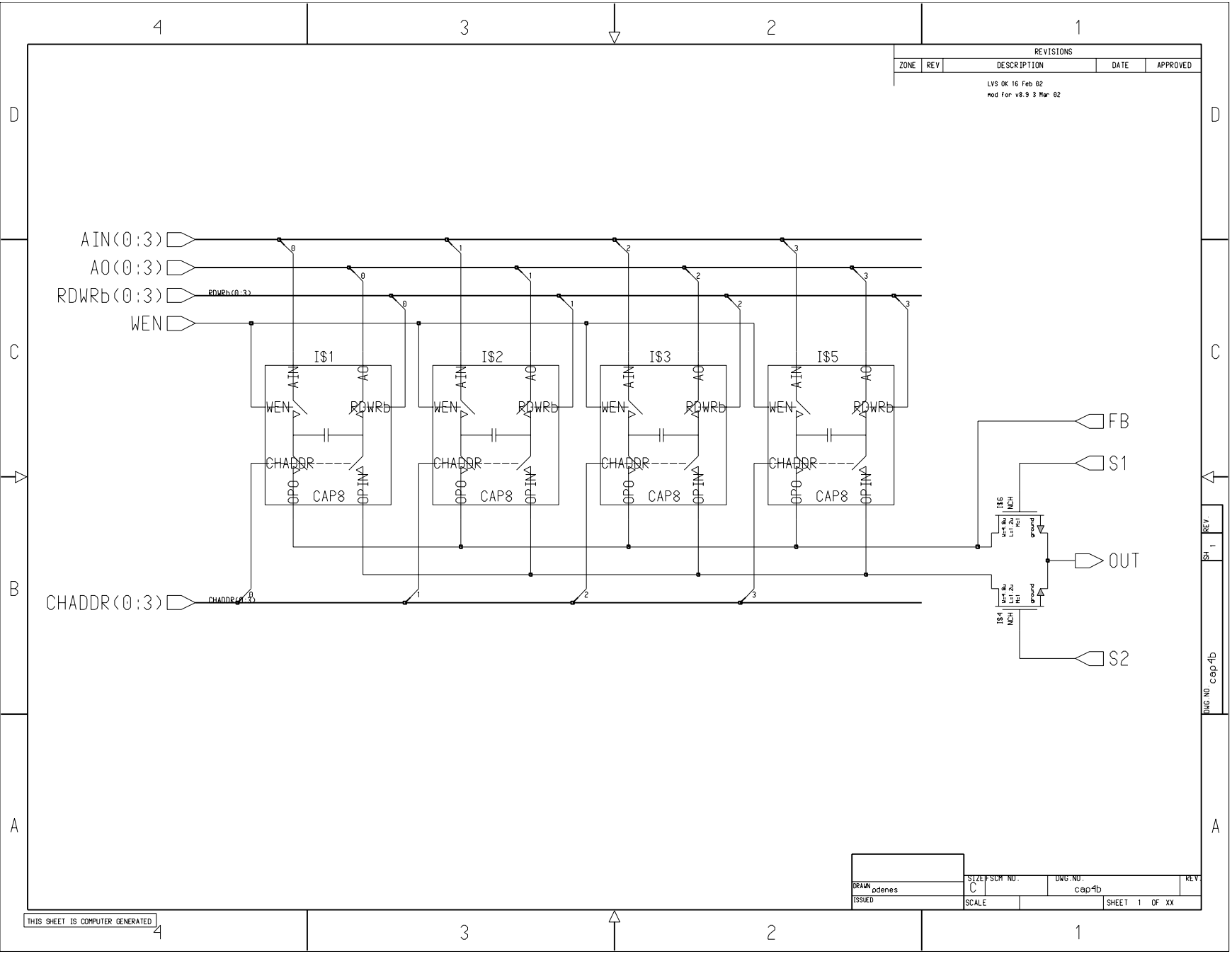
LVS OK 16 Feb 02



DRAWN pdenes	SIZE B	FSCM NO.	DWG.NO. bit3	REV.
ISSUED	SCALE		SHEET 1 OF XX	

THIS SHEET IS COMPUTER GENERATED

Design Pathname	Version	Edited By	Last Edit
/home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch/bit3 schematic sheet1	1	pdenes	Saturday, February 16, 2002, 5:57:32 pm

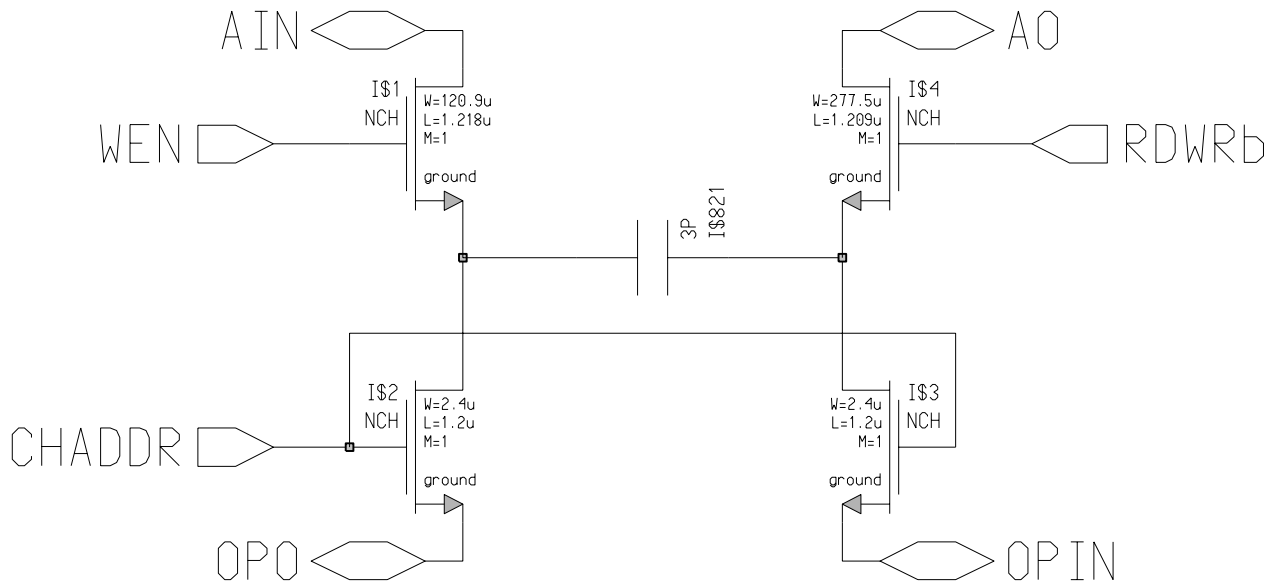


Design Pathname	Version	Edited By	Last Edit
/home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch/cap4b schematic sheet1	1	pdenes	Saturday, February 16, 2002, 7:14:53 pm

DWG.NO cap8	SH 1	REV.

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

LVS OK 25JAN01
mod v8.9 3 Mar 02



NMOS dimensions are a bit funny because of the way the transistors are drawn

DRAWN pdenes	SIZE A	FSCM NO.	DWG.NO. cap8	REV.
ISSUED	SCALE		SHEET 1 OF XX	

THIS SHEET IS COMPUTER GENERATED

Design Pathname:	Version:	Edited By:	Last Edit:
/home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch/cap8 schematic sheet1	1	pdenes	Friday, January 25, 2002, 8:19:18 am

Inverter Table (for inverters in ATWR5)
==========
All transistors have L=1.2u

invXXX	W(p)	W(n)
9	21.6	10.8
6a	12	7.2
6	14.4	7.2
48	115.2	57.6
40	96	48
4	9.6	4.8
3	7.2	4.8
2	2.4	2.4
18	43.2	21.6
16	38.4	19.2
12	24	14.4
10x9	192	96
10x4p5	96	48

```
                  ##################################################
                  ##                                              ##
                  ##         C A L I B R E   S Y S T E M          ##
                  ##                                              ##
                  ##             L V S   R E P O R T              ##
                  ##                                              ##
                  ##################################################


REPORT FILE NAME:         /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/lvs.rep
LAYOUT NAME:              /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/pdATWR/ATWR5
SOURCE NAME:              /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/ATWR5/default
RULE FILE:                /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/ORB12v89.ext
LVS MODE:                 Mask
RULE FILE NAME:           /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/ORB12v89.ext
CREATION TIME:            Mon Mar  4 08:28:57 2002
CURRENT DIRECTORY:        /home/engfile2/did/pdenes/IceCube/ATWD/menATWR
USER NAME:                pdenes

*************************************************************************************************
                              OVERALL COMPARISON RESULTS
*************************************************************************************************


                       #       ###################       _   _
                      #        #                 #       *   *
                  #   #        #     CORRECT     #         |
                   # #         #                 #       \___/
                    #          ###################


  Warning:  Unbalanced smashed mosfets were matched.
  Warning:  Ambiguity points were found and resolved arbitrarily.

-------------------------------------------------------------------------------------------------

INITIAL NUMBERS OF OBJECTS
```

```
--------------------------

                Layout    Source         Component Type
                ------    ------         --------------
 Nets:           11149     11148    *

 Instances:      17129     13290    *    mn (3 pins)
                 13116     10363    *    mp (4 pins)
                   641       641         c (2 pins)
                    12        12         r (2 pins)
                    50        50         pad (1 pins)
                ------    ------
 Total Inst:     30948     24356


NUMBERS OF OBJECTS AFTER TRANSFORMATION
---------------------------------------

                Layout    Source         Component Type
                ------    ------         --------------
 Nets:           10733     10733

 Instances:      13003     13003         mn (3 pins)
                  9815      9815         mp (4 pins)
                   641       641         c (2 pins)
                    12        12         r (2 pins)
                    50        50         pad (1 pins)
                ------    ------
 Total Inst:     23521     23521


       * = Number of objects in layout different from number in source.


*****************************************************************************************************
                                       LVS PARAMETERS
*****************************************************************************************************


o LVS Setup:

   Component Type Properties:             element
   Subtype Property:                      subtype
```

```
/home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/ATWR5
(schm:schematic)
   $MGC_GENLIB/ground (primitive)
   /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/pad (primitive)
   /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/cker
(schm:schematic)
      $MGC_GENLIB/portin (primitive)
      $MGC_GENLIB/portbi (primitive)
      $MGC_GENLIB/portout (primitive)
      /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/hclock
(schm:schematic)
         $MGC_GENLIB/portin (primitive)
         $MGC_GENLIB/portout (primitive)
         $MGC_GENLIB/portbi (primitive)
         /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/inv10x4p5
(schm:schematic)
            $MGC_GENLIB/portbi (primitive)
            $MGC_GENLIB/portin (primitive)
            $MGC_GENLIB/portout (primitive)
            $MGC_IC_DEVICE_LIB/nmos_3pin (primitive)
            /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/pmos_
4pin (primitive)
         /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/inv10x9
(schm:schematic)
            $MGC_GENLIB/portbi (primitive)
            $MGC_GENLIB/portin (primitive)
            $MGC_GENLIB/portout (primitive)
            $MGC_IC_DEVICE_LIB/nmos_3pin (primitive)
            /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/pmos_
4pin (primitive)
         /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/nor4p5
(schm:schematic)
            $MGC_GENLIB/portin (primitive)
            $MGC_GENLIB/portout (primitive)
            $MGC_GENLIB/portbi (primitive)
            $MGC_IC_DEVICE_LIB/nmos_3pin (primitive)
            /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/pmos_
4pin (primitive)
         /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/inv18
(schm:schematic)
            $MGC_GENLIB/portbi (primitive)
            $MGC_GENLIB/portin (primitive)
            $MGC_GENLIB/portout (primitive)
            $MGC_IC_DEVICE_LIB/nmos_3pin (primitive)
            /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/pmos_
4pin (primitive)
      /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/inv9
(schm:schematic)
         $MGC_GENLIB/portbi (primitive)
         $MGC_GENLIB/portin (primitive)
         $MGC_GENLIB/portout (primitive)
         $MGC_IC_DEVICE_LIB/nmos_3pin (primitive)
         /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/pmos_4pin
(primitive)
```

```
   /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/pdAUX
(schm:schematic)
      $MGC_GENLIB/portin (primitive)
      $MGC_GENLIB/portout (primitive)
      $MGC_GENLIB/portbi (primitive)
      /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/nand2a
(schm:schematic)
         $MGC_IC_DEVICE_LIB/nmos_3pin (primitive)
         $MGC_GENLIB/portbi (primitive)
         $MGC_GENLIB/portin (primitive)
         $MGC_GENLIB/portout (primitive)
         /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/pmos_4pin
(primitive)
      /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/inv40
(schm:schematic)
         $MGC_GENLIB/portbi (primitive)
         $MGC_GENLIB/portin (primitive)
         $MGC_GENLIB/portout (primitive)
         $MGC_IC_DEVICE_LIB/nmos_3pin (primitive)
         /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/pmos_4pin
(primitive)
      /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/nand3a
(schm:schematic)
         $MGC_GENLIB/portbi (primitive)
         $MGC_GENLIB/portout (primitive)
         $MGC_GENLIB/portin (primitive)
         $MGC_IC_DEVICE_LIB/nmos_3pin (primitive)
         /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/pmos_4pin
(primitive)
   /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/pdBIAS
(schm:schematic)
      $MGC_GENLIB/portin (primitive)
      $MGC_GENLIB/portout (primitive)
      /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/pmos_4pin
(primitive)
      $MGC_IC_DEVICE_LIB/nmos_3pin (primitive)
      $MGC_IC_DEVICE_LIB/ideal_capacitor (primitive)
   /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/cbits
(schm:schematic)
      $MGC_GENLIB/portin (primitive)
      $MGC_GENLIB/portbi (primitive)
      $MGC_GENLIB/portout (primitive)
      /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/cbit4
(schm:schematic)
         $MGC_GENLIB/portin (primitive)
         $MGC_GENLIB/portout (primitive)
         $MGC_GENLIB/portbi (primitive)
         /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/tgate
(schm:schematic)
            $MGC_GENLIB/portbi (primitive)
            $MGC_GENLIB/portin (primitive)
            /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/pmos_
4pin (primitive)
            $MGC_IC_DEVICE_LIB/nmos_3pin (primitive)
```

```
         /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/inv4
(schm:schematic)
            $MGC_GENLIB/portbi (primitive)
            $MGC_GENLIB/portin (primitive)
            $MGC_GENLIB/portout (primitive)
            $MGC_IC_DEVICE_LIB/nmos_3pin (primitive)
            /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/pmos_
4pin (primitive)
         /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/inv16
(schm:schematic)
            $MGC_GENLIB/portbi (primitive)
            $MGC_GENLIB/portin (primitive)
            $MGC_GENLIB/portout (primitive)
            $MGC_IC_DEVICE_LIB/nmos_3pin (primitive)
            /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/pmos_
4pin (primitive)
         /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/inv48
(schm:schematic)
            $MGC_GENLIB/portbi (primitive)
            $MGC_GENLIB/portin (primitive)
            $MGC_GENLIB/portout (primitive)
            $MGC_IC_DEVICE_LIB/nmos_3pin (primitive)
            /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/pmos_
4pin (primitive)
         /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/pmos_4pin
(primitive)
      /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/cbit3
(schm:schematic)
         $MGC_GENLIB/portbi (primitive)
         $MGC_GENLIB/portout (primitive)
         $MGC_GENLIB/portin (primitive)
         /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/inv48
(schm:schematic)
            $MGC_GENLIB/portbi (primitive)
            $MGC_GENLIB/portin (primitive)
            $MGC_GENLIB/portout (primitive)
            $MGC_IC_DEVICE_LIB/nmos_3pin (primitive)
            /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/pmos_
4pin (primitive)
         /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/inv16
(schm:schematic)
            $MGC_GENLIB/portbi (primitive)
            $MGC_GENLIB/portin (primitive)
            $MGC_GENLIB/portout (primitive)
            $MGC_IC_DEVICE_LIB/nmos_3pin (primitive)
            /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/pmos_
4pin (primitive)
         /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/inv4
(schm:schematic)
            $MGC_GENLIB/portbi (primitive)
            $MGC_GENLIB/portin (primitive)
            $MGC_GENLIB/portout (primitive)
            $MGC_IC_DEVICE_LIB/nmos_3pin (primitive)
            /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/pmos_
```

```
4pin (primitive)
         /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/tgate
(schm:schematic)
            $MGC_GENLIB/portbi (primitive)
            $MGC_GENLIB/portin (primitive)
            /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/pmos_
4pin (primitive)
            $MGC_IC_DEVICE_LIB/nmos_3pin (primitive)
         /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/inv6
(schm:schematic)
            $MGC_GENLIB/portbi (primitive)
            $MGC_GENLIB/portin (primitive)
            $MGC_GENLIB/portout (primitive)
            $MGC_IC_DEVICE_LIB/nmos_3pin (primitive)
            /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/pmos_
4pin (primitive)
         /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/pmos_4pin
(primitive)
         $MGC_IC_DEVICE_LIB/nmos_3pin (primitive)
      /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/cbit2
(schm:schematic)
         $MGC_GENLIB/portbi (primitive)
         $MGC_GENLIB/portout (primitive)
         $MGC_GENLIB/portin (primitive)
         /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/tgate
(schm:schematic)
            $MGC_GENLIB/portbi (primitive)
            $MGC_GENLIB/portin (primitive)
            /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/pmos_
4pin (primitive)
            $MGC_IC_DEVICE_LIB/nmos_3pin (primitive)
         /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/inv48
(schm:schematic)
            $MGC_GENLIB/portbi (primitive)
            $MGC_GENLIB/portin (primitive)
            $MGC_GENLIB/portout (primitive)
            $MGC_IC_DEVICE_LIB/nmos_3pin (primitive)
            /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/pmos_
4pin (primitive)
         /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/inv16
(schm:schematic)
            $MGC_GENLIB/portbi (primitive)
            $MGC_GENLIB/portin (primitive)
            $MGC_GENLIB/portout (primitive)
            $MGC_IC_DEVICE_LIB/nmos_3pin (primitive)
            /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/pmos_
4pin (primitive)
         /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/inv4
(schm:schematic)
            $MGC_GENLIB/portbi (primitive)
            $MGC_GENLIB/portin (primitive)
            $MGC_GENLIB/portout (primitive)
            $MGC_IC_DEVICE_LIB/nmos_3pin (primitive)
            /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/pmos_
```

```
4pin (primitive)
         /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/inv6
(schm:schematic)
            $MGC_GENLIB/portbi (primitive)
            $MGC_GENLIB/portin (primitive)
            $MGC_GENLIB/portout (primitive)
            $MGC_IC_DEVICE_LIB/nmos_3pin (primitive)
            /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/pmos_
4pin (primitive)
         /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/pmos_4pin
(primitive)
      /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/inv6
(schm:schematic)
         $MGC_GENLIB/portbi (primitive)
         $MGC_GENLIB/portin (primitive)
         $MGC_GENLIB/portout (primitive)
         $MGC_IC_DEVICE_LIB/nmos_3pin (primitive)
         /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/pmos_4pin
(primitive)
   $MGC_IC_DEVICE_LIB/ideal_resistor (primitive)
   /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/pdCORE
(schm:schematic)
      $MGC_GENLIB/portin (primitive)
      $MGC_GENLIB/portout (primitive)
      /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/trigger
(schm:schematic)
         $MGC_GENLIB/portbi (primitive)
         $MGC_GENLIB/portin (primitive)
         $MGC_GENLIB/portout (primitive)
         /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/ll
(schm:schematic)
            $MGC_GENLIB/portin (primitive)
            $MGC_GENLIB/portbi (primitive)
            $MGC_GENLIB/portout (primitive)
            /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/pmos_
4pin (primitive)
            $MGC_IC_DEVICE_LIB/nmos_3pin (primitive)
            /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/zd7
(schm:schematic)
               $MGC_GENLIB/portbi (primitive)
               $MGC_GENLIB/portin (primitive)
               $MGC_GENLIB/portout (primitive)
               $MGC_IC_DEVICE_LIB/nmos_3pin (primitive)
               /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/pmos_
4pin (primitive)
         /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/zd128
(schm:schematic)
            $MGC_GENLIB/portout (primitive)
            $MGC_GENLIB/portbi (primitive)
            $MGC_GENLIB/portin (primitive)
            /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/zd16
(schm:schematic)
               $MGC_GENLIB/rip (primitive)
               $MGC_GENLIB/portin (primitive)
```

```
                $MGC_GENLIB/portout (primitive)
                $MGC_GENLIB/portbi (primitive)
                /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/zd7
(schm:schematic)
                   $MGC_GENLIB/portbi (primitive)
                   $MGC_GENLIB/portin (primitive)
                   $MGC_GENLIB/portout (primitive)
                   $MGC_IC_DEVICE_LIB/nmos_3pin (primitive)

/home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/pmos_4pin
(primitive)
          /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/lander
(schm:schematic)
             $MGC_GENLIB/portbi (primitive)
             $MGC_GENLIB/portin (primitive)
             $MGC_GENLIB/portout (primitive)
             /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/pmos_
4pin (primitive)
             $MGC_IC_DEVICE_LIB/nmos_3pin (primitive)
          $MGC_IC_DEVICE_LIB/nmos_3pin (primitive)
       /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/slice3
(schm:schematic)
          $MGC_GENLIB/portin (primitive)
          $MGC_GENLIB/portout (primitive)
          $MGC_GENLIB/portbi (primitive)
          /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/bit3
(schm:schematic)
             $MGC_GENLIB/portout (primitive)
             $MGC_GENLIB/portbi (primitive)
             $MGC_GENLIB/portin (primitive)
             $MGC_GENLIB/ground (primitive)
             /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/tgate2
(schm:schematic)
                $MGC_GENLIB/portbi (primitive)
                $MGC_GENLIB/portin (primitive)
                /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/pmos_
4pin (primitive)
                $MGC_IC_DEVICE_LIB/nmos_3pin (primitive)
             /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/inv3
(schm:schematic)
                $MGC_GENLIB/portbi (primitive)
                $MGC_GENLIB/portin (primitive)
                $MGC_GENLIB/portout (primitive)
                $MGC_IC_DEVICE_LIB/nmos_3pin (primitive)
                /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/pmos_
4pin (primitive)
             /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/inv2
(schm:schematic)
                $MGC_GENLIB/portbi (primitive)
                $MGC_GENLIB/portin (primitive)
                $MGC_GENLIB/portout (primitive)
                $MGC_IC_DEVICE_LIB/nmos_3pin (primitive)
                /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/pmos_
4pin (primitive)
```

```
         /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/comp6
(schm:schematic)
            $MGC_GENLIB/portout (primitive)
            $MGC_GENLIB/portbi (primitive)
            $MGC_GENLIB/portin (primitive)
            $MGC_GENLIB/ground (primitive)
            $MGC_IC_DEVICE_LIB/nmos_3pin (primitive)
            /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/nand4
(schm:schematic)
               $MGC_IC_DEVICE_LIB/nmos_3pin (primitive)
               $MGC_GENLIB/portbi (primitive)
               $MGC_GENLIB/portin (primitive)
               $MGC_GENLIB/portout (primitive)
               /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/pmos_
4pin (primitive)
            /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/nand2
(schm:schematic)
               $MGC_IC_DEVICE_LIB/nmos_3pin (primitive)
               $MGC_GENLIB/portin (primitive)
               $MGC_GENLIB/portout (primitive)
               $MGC_GENLIB/portbi (primitive)
               /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/pmos_
4pin (primitive)
            /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/inv12
(schm:schematic)
               $MGC_GENLIB/portbi (primitive)
               $MGC_GENLIB/portin (primitive)
               $MGC_GENLIB/portout (primitive)
               $MGC_IC_DEVICE_LIB/nmos_3pin (primitive)
               /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/pmos_
4pin (primitive)
            /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/inv6a
(schm:schematic)
               $MGC_GENLIB/portbi (primitive)
               $MGC_GENLIB/portin (primitive)
               $MGC_GENLIB/portout (primitive)
               $MGC_IC_DEVICE_LIB/nmos_3pin (primitive)
               /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/pmos_
4pin (primitive)
            /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/pmos_
4pin (primitive)
         /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/cap4b
(schm:schematic)
            $MGC_GENLIB/rip (primitive)
            $MGC_GENLIB/portin (primitive)
            $MGC_GENLIB/portout (primitive)
            /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/cap8
(schm:schematic)
               $MGC_GENLIB/portin (primitive)
               $MGC_GENLIB/portbi (primitive)
               $MGC_IC_DEVICE_LIB/nmos_3pin (primitive)
               $MGC_IC_DEVICE_LIB/ideal_capacitor (primitive)
            $MGC_IC_DEVICE_LIB/nmos_3pin (primitive)
         /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/opa5
```

```
(schm:schematic)
            $MGC_GENLIB/portin (primitive)
            $MGC_GENLIB/portbi (primitive)
            $MGC_GENLIB/ground (primitive)
            $MGC_GENLIB/portout (primitive)
            $MGC_IC_DEVICE_LIB/nmos_3pin (primitive)
            /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/pmos_
4pin (primitive)
         $MGC_IC_DEVICE_LIB/ideal_capacitor (primitive)
   /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/zpadin3
(schm:schematic)
      $MGC_GENLIB/portout (primitive)
      $MGC_GENLIB/portbi (primitive)
      /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/pad
(primitive)
      /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/pmos_4pin
(primitive)
      $MGC_IC_DEVICE_LIB/nmos_3pin (primitive)
      $MGC_IC_DEVICE_LIB/ideal_resistor (primitive)
   /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/zpadts
(schm:schematic)
      $MGC_GENLIB/portbi (primitive)
      $MGC_GENLIB/portin (primitive)
      $MGC_IC_DEVICE_LIB/nmos_3pin (primitive)
      /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/pmos_4pin
(primitive)
      /home/engfile2/did/pdenes/IceCube/ATWD/menATWR/sch2/pad
(primitive)
```