Analog Transient Waveform Digitizer R1.1 (V2)

Chip design by Stuart A. Kleinfelder
Manual by Gerald T. Przybylski
Lawrence Berkeley National Laboratory
Physics Division, KM^3 working group
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1 General Description

This Analog Transient Waveform Digitizer ASIC design addresses the problem of capturing fast transient waveforms of modest duration with miserly power consumption. The design meets the speed and power requirements without the need to resort to exotic manufacturing processes (the chip was manufactured on the Orbit Semiconductor Forsight 1.2 micron fabrication line). This version, version 3, incorporates an array of analog to digital converters, one to a time sample, which convert all the samples in a selected input channel at once. On-chip parallel conversion reduces the complexity of readout hardware and eliminates the need for a great deal of precision off-chip analog circuitry. The chip incorporates isolation structures to electrically separate analog and digital circuitry.

1.1 Theory of Operation

When triggered, the Analog Transient Waveform Digitizer IC, depicted in figure 1, captures four channels of waveform to four corresponding banks of 128 capacitors. FET switches between the input and each capacitor are closed and opened in rapid succession forming a sampling window that travels down the row of sample storage capacitors.

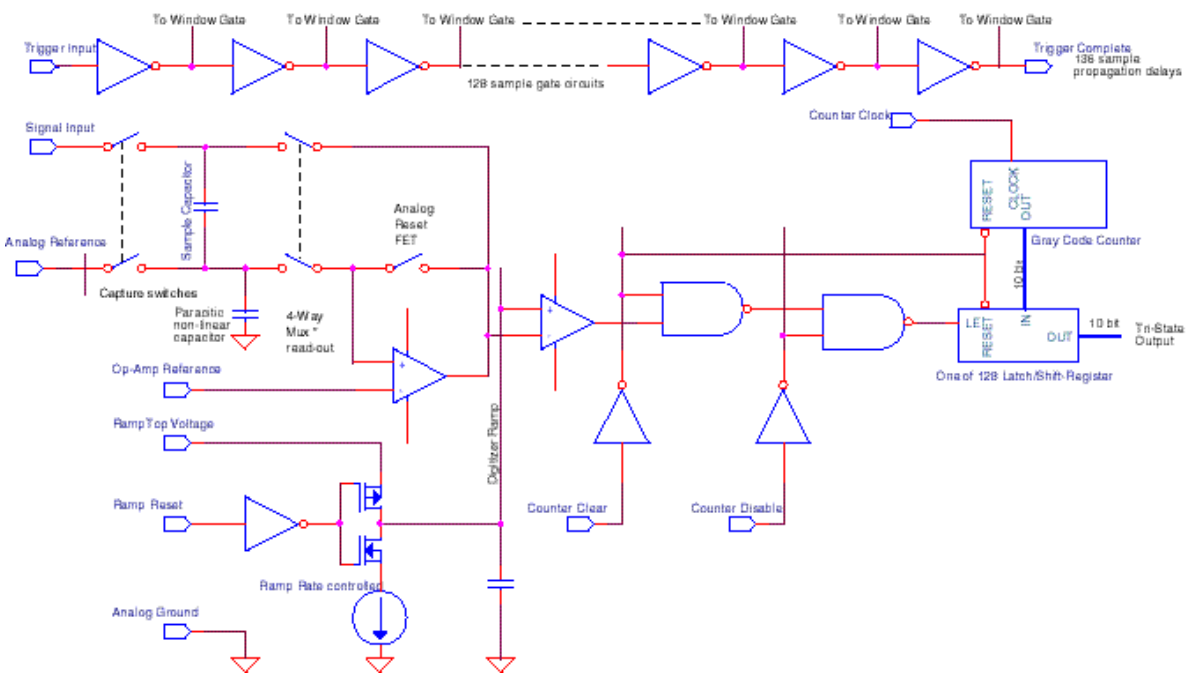


Figure 1~~1~~. Essential elements of the ATWD design concept

Stuart Kleinfelder's thesis describes the technology in detail. A variable control current applied to the *Trigger Bias* input adjusts the capture rate over a range of about 0.3 to a maximum of around 2 gigasamples per second. In acquisition mode, the sample capacitor is connected by FET switches to the analog input during the sampling window. The resistance of the FET switches times the sampling capacitance gives a time constant which must be small with respect to the capture window duration. The sampling window width for this version of ATWD is four times the sampling period. The capacitor arrays retain the waveform until digitized.

Stuart Armin Kleinfelder, A Multi-Gigahertz Analog Transient Recorder Integrated Circuit, May, 1992, University of California, Berkeley, Department of Electrical Engineering and Computer Science.

The FET switch between the *Analog Reference* pin and the sample capacitor has the smallest series resistance when the *Analog Reference* voltage is near ground. The resistance of that n-MOS switch goes up dramatically as the *Analog Reference voltage* raises above about 3.5V. Since the buffer amplifier and comparator are not rail-to-rail designs, one must choose an *Op-Amp Reference* voltage compatible with the *Analog Reference* voltage. If *Analog Reference* and *Op-Amp Reference* are set to the same voltage, then the buffer output voltage will equal the input signal voltage stored on the capacitor. The output of the buffer will be level shifted by the difference between the *Analog Reference* and *Op-Amp Reference* voltages. Furthermore, if level shifting occurs, charge must be transferred into the non-linear parasitic capacitor at the bottom of the sample capacitor.

In digitize mode, the sample capacitor is connected to the buffer amplifier only during the digitizing phase. The stored analog signal samples are digitized by a single bank of 128 ten bit Wilkinson common ramp ADCs arranged one to one with the storage capacitor bank. A four-way readout multiplexer routes the selected capacitor bank to the buffer amplifier/digitizer array. Closing the buffer amplifier shunting FET while reading out will obliterate the previous sample. This technique may be useful where maximum precision is required.

Each digitizer consists of a comparator and a counter. Conversion commences with the application of a ramp voltage to the comparator coincident with the application of a pulse train to the Gray code counter. When the comparator detects a threshold crossing it causes the counter to latch its current value. The counters are merged with the output shift register structure. Shift clock pulses move the data to the ten bit wide tri-state output bus. One datum is transferred to the output bus per shift clock cycle. The last time sample taken is delivered to the output bus first.

1.2 Pin Configuration

The pin-out, figure 2, shows the arrangement of the ATWD die bonding pads and the names associated with them. This chip may be mounted on a carrier and installed in a socket, or bonded directly to a printed circuit board. Data output and output enable pads line one side of the chip. Logic control inputs line the opposite side of the chip. Signal inputs enter one end of the chip, and analog reference and control voltages and currents enter the other end of the chip. Figure 3 details die size, pad locations and pitches to facilitate the layout for chip-on-board designs or for bonding to a carrier.

1.3 Application

Figure 4 depicts a typical implementation of the ATWD chip. The current source inputs are current mirrors, therefore, they are relatively immune to the voltage present at the input node. Resistors may be used to program the bias current inputs without fear of restricting the operating range of any internal circuit. Each current control input is protected by a parasitic diode to a power supply rail or ground, depending on polarity.

All digital inputs are C-MOS. Digital inputs are protected by back biased diodes to the plus and minus rails. (The diodes are parasitic, artifacts of the cell structure). None of the protective diodes is robust in nature. ESD suppression precautions must be taken while handling the dice or carrier mounted dice. Transient resistant application circuit design must also be implemented. The digital inputs have series input resistors to enhance their resistance to ESD. The analog inputs (signal inputs) require robust protection from damage by signal sources. For instance, photomultiplier tubes are particularly capable of causing damage.

[2] At present, the effects of the parasitic capacitor on the signal are unknown. Neither modeling nor actual measurements yet exist. (6/26/98 gtp)

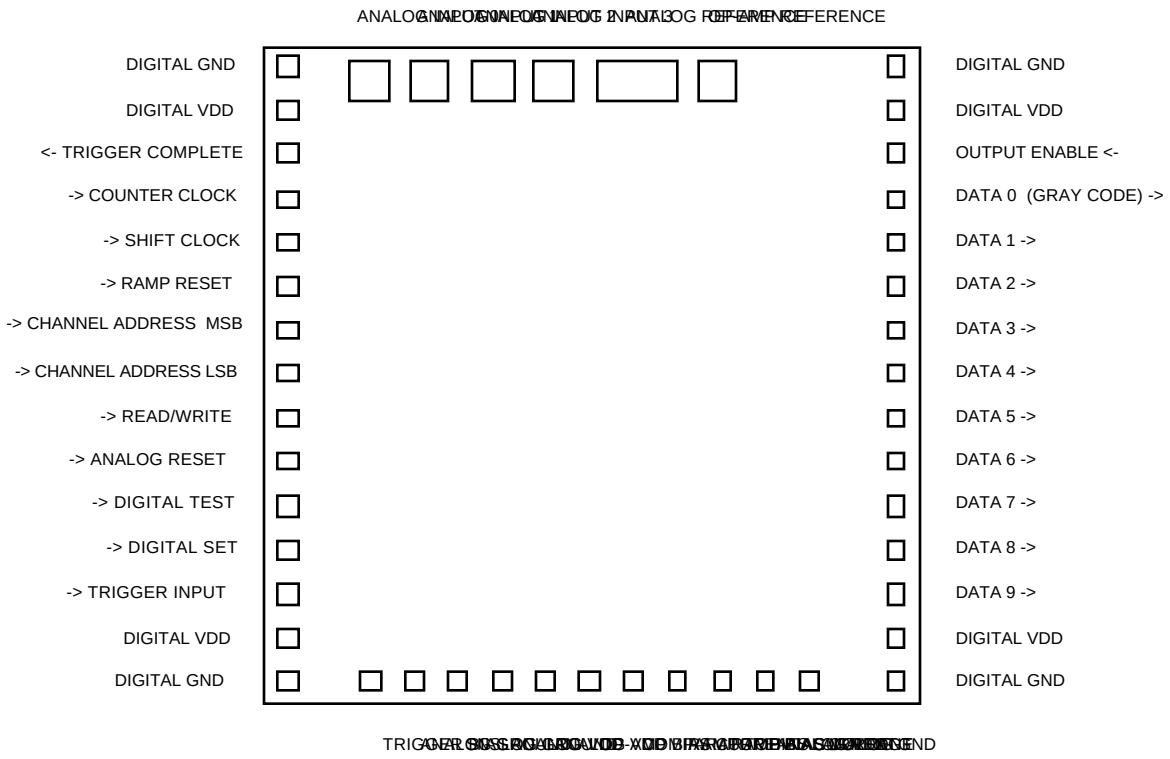


Figure 2~~2~~ ATWD die pad to signal name mapping. Arrow (->) pointing toward chip indicates digital input, arrow pointing away from chip indicate digital output

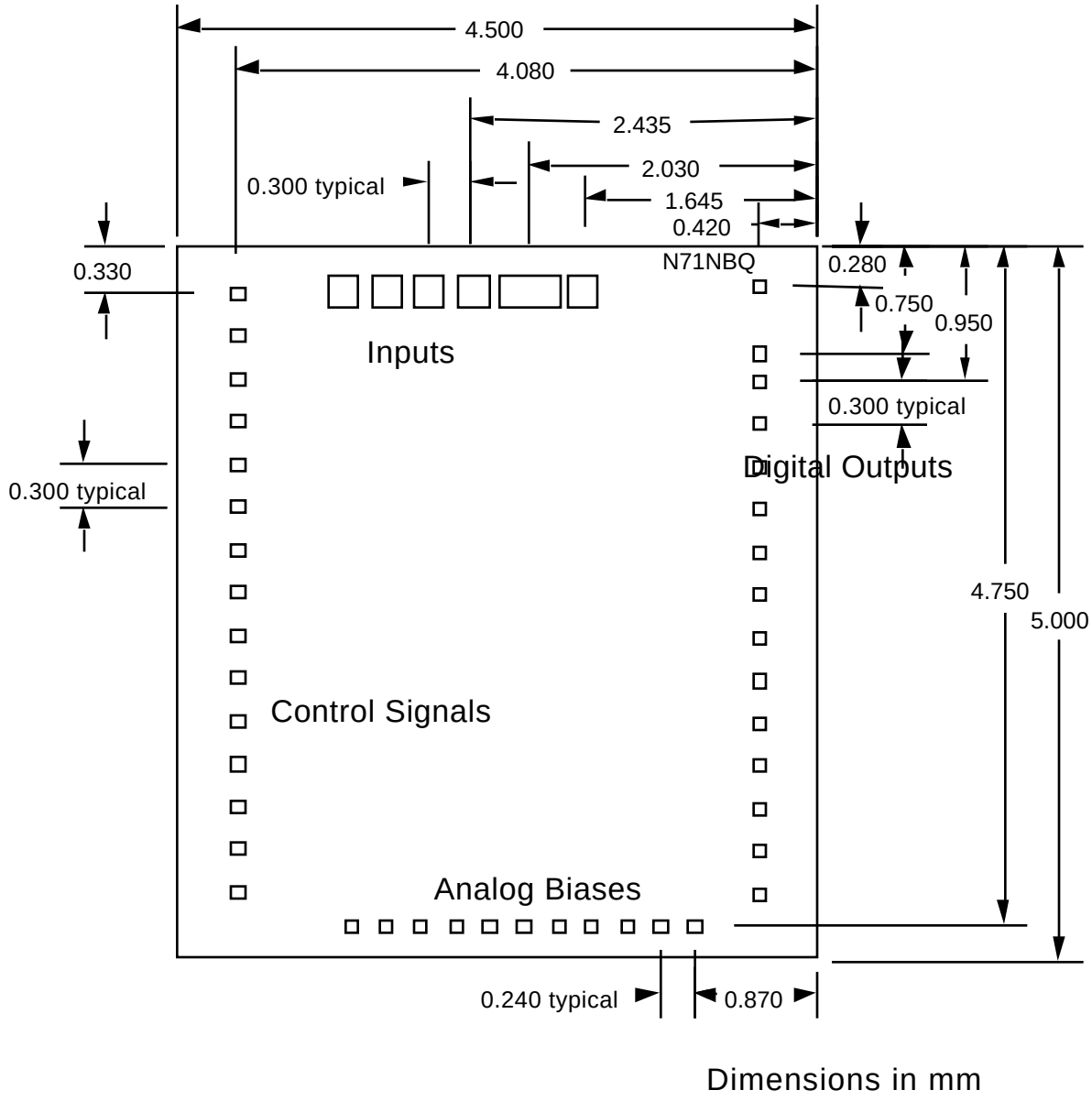


Figure 3~~3~~. ATWD Die pad locations. R1.1 April 7, 1998 gtp

The ATWD design does not provide any internal power supply current limiting or latch-up protection. External power limiting is recommended, as is some provision for power-off reset to recover from latch-up.

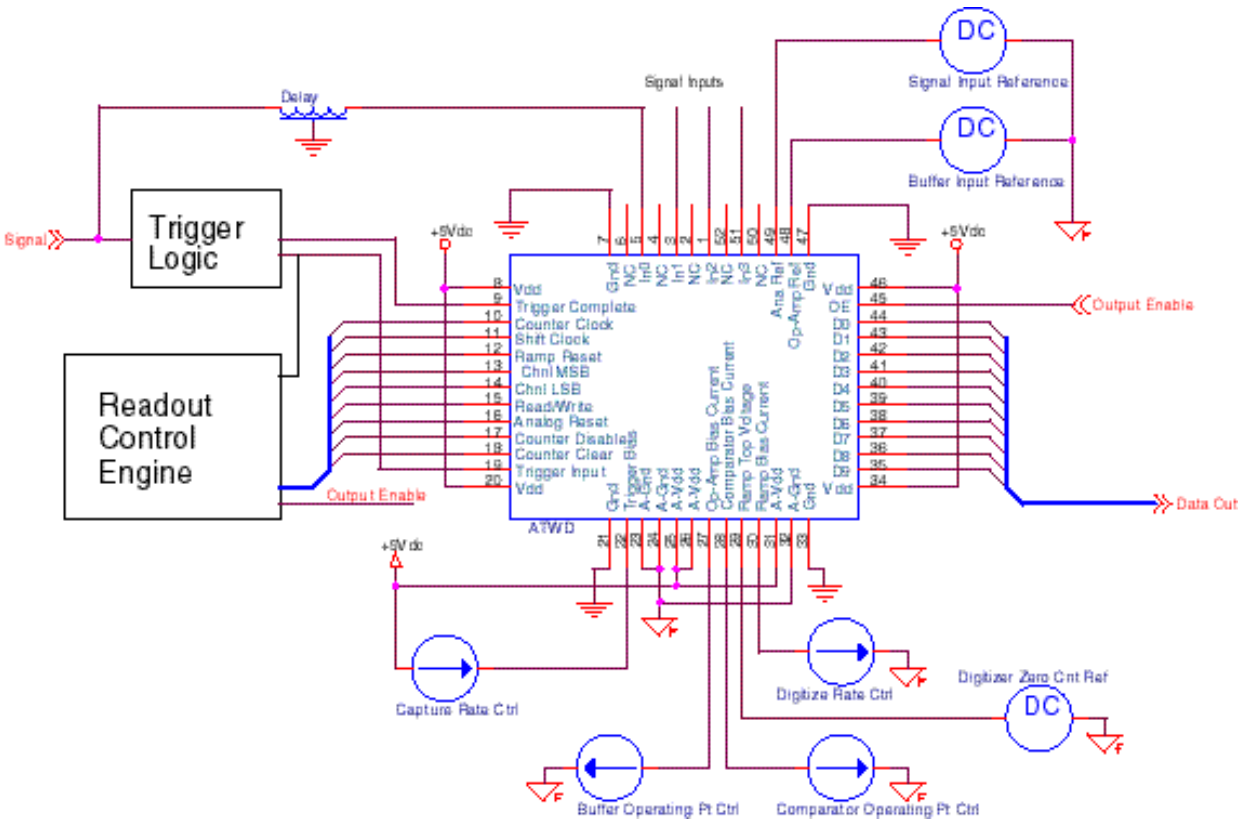


Figure 44 The typical ATWD implementation.

The *Analog Reference* input is switched to the lower end of the sampling capacitor during signal acquisition. The impedance of the source connected to the *Analog Reference* pin must be low at the highest input frequency the input is expected to see. Operation at or near Analog Ground should result in widest bandwidth and input range. A non-linear parasitic capacitance exists between the bottom of the sample capacitor and Analog Ground. The input amplifier will cause the lower end of the sample capacitor to slue to the *Op-Amp Reference* voltage. This will transfer charge into this parasitic capacitor. The input amplifier cannot be operated with zero volts applied to the *Op-Amp Reference.* Therefore, it is recommended that the *Op-Amp Reference* and *Analog Reference* both be operated at the same voltage between 0.7V and 3V with respect to Analog Ground

The rising edge of *Trigger* ripples down an array of inverters (tapped digital delay line) feeding the sample window forming logic. The last inverter in the chain delivers its output to the *Trigger Complete* pin. The falling edge of *Trigger Complete* indicates the end of the signal acquisition process. Higher *Trigger Bias* current cases more rapid propagation. The *Trigger* high to *Trigger Complete* low propagation time spans the sampling period. The window forming logic uses a four-stage look-ahead. Four extra delay stages exist between the last capture gate and the trigger complete output driver. Consequently, the *Trigger Complete* must propagate through 136 delay stages before appearing at *Trigger Complete.* Hence,

$$TotalDelay = (136x\ SampleRate) + (SeveralGateDelays)$$

Furthermore, the capture aperture width depends on the capture rate (*Trigger bias)* as well.

The delay chain consists of inverter pairs. The inverters are not identical. The controlled inverter has speed control implemented in one leg of the totem-pole. Reducing the control current slows the propagation of the leading edge of the *Trigger* signal through the delay chain. The trailing edge of *Trigger Complete* propagates at a fixed rate. ATWD sample rate is controlled by applying a bias current to the *Capture Rate* input. The bias can be fixed, or controlled with a delay-locked loop. For a delay-lock loop, the phase of the falling edge of *Trigger Complete* with respect to a known delay gives the error signal. When *Trigger Complete* leads the reference delay, the *Trigger Bias* should be reduced. *Trigger* must remain high until Trigger Complete goes low.

The falling edge of *Trigger* initiates capture circuit reset. Setting the *Trigger* low before a high appears at *Trigger Complete* will cause premature termination of the capture operation. The digitizing sequence may begin at any time after *Trigger Complete* goes low, or not at all in the case that the captured event is abandoned. If readout is not

initiated, new triggers should be precluded until *Trigger Complete* goes high.

Adjusting *Trigger Bias* on an event by event basis is not recommended and has not been tested.

The resistance of the FET switches is finite. The bonding wires have inductance as well. The time constant of the FET resistance and the charge storage capacitor and the inductance must be short compared to the capture aperture to insure that the sample is accurate to the required precision. They also set the bandwidth limit on the device. The bond wire inductance can be reduced bonding multiple wires from the (oversized) pads to the circuit or carrier. At very high sampling rates the charge left on the sampling capacitor from the last event may not equalize with the signal source. If there is evidence that remembered charge contributes to amplitude error, the charge can be bled off by transferring it to the shorted buffer amplifier.

The input buffer amplifier for the analog to digital converter consists of a unity gain operational amplifier driving the non-inverting port of a comparator. The buffer amplifier non-inverting input is referenced to fixed DC bias. Switching the sampling capacitor between the output and the inverting input of the op-amp transfers the capacitor voltage to the comparator input. Any voltage present between the input and output of the op-amp before switching the sample capacitor terminals to the introduces an error. Therefore, a FET switch activated by the *Analog Reset* line shorts the op-amp output to the input, bleeding off undesirable charge. Care should be taken to minimize the amount of time the input amplifier is allowed to “float”. The amplifier floats when both *Analog Reset* and *Read/Write* are both low. The buffer amplifier must not be ~~allowe~~d to float during *Trigger* as performance is severely degraded by charge injected into the unshorted buffer circuit. Each op-amp and comparator in the ADC array has its own offset and offset drift due to temperature effects and leakage currents.

Analog Reset low should not overlap *Read/Write* high before digitizing since this will drain charge from the sample capacitor before it can be sampled. Explicitly discharging the sample capacitor before the next trigger may improve system precision.

The operating current of the Op-Amp and Comparator determine the gain, gain-bandwidth product, noise, settling time, and linear range. More current results in a faster, lower noise, lower gain buffer. Excessive current restricts the “head-room”. Excessive current will cause the stages to malfunction. The transition from normal operation to malfunction is abrupt as current increases beyond a threshold. Low stage current gives more gain and linearity as well as longer settling time.

The ADC ramp sweeps *from Ramp Top Voltage* toward *Analog Ground*. Signal input voltage cannot exceed *Ramp Top Voltage*. *Ramp Top Voltage* must be negative with respect to *Analog Reference*. The ADC Gray code counter counts forward from zero as the ADC comparator voltage ramps at a constant rate toward zero volts.. Consequently, more positive input voltages produce lower ADC counts. The ADC counter will not count properly if *Shift Clock* is held high during the digitizing. This is a consequence of the fact that the shift register functionality is merged with the latch functionality. The ADC counter increments on both positive and negative edges of *Counter Clock*. Counting commences with the first *Counter Clock* edge after *Counter Disable* goes low. The application of 1024 or more *Counter Clock* edges (512 full cycles) will cause the ADC counter to wrap around to zero counts and continue counting.

Ramp Bias current controls the ramp rate. Higher current corresponds to faster ramp rate. The ADC ramp rate must be adjusted to sweep through the input range in the time it takes to count 1023 *Counter Clock* edges (if full system resolution is desired). Faster, lower resolution data may be acquired by increasing the ramp rate in proportion to the decrease in the number of *Counter Clock* edges. Each bit of resolution lost reduces the digitizing time by half. The ramp rate may be left fixed if one desires to only digitize the first part of the ADC span.

It may be possible to bus the *Ramp Top Voltage* inputs of several ATWD chips together depending on the uniformity of the chips. *Analog Reference, Op-Amp Reference* and the spatial noise pattern of the digitizer channels primarily dictate the choice *Ramp Top Voltage*. One should not assume that the *Ramp Top Voltage* may be ganged. It may be desirable to share *Analog Reference* and *Op-Amp Reference* among several ATWDs. No data is yet available to justify or preclude this approach.

Counter Disable must remain low while data is shifted to the host system. Once digitization is complete the transfer of data out of the ATWD may commence immediately, or may be delayed indefinitely. The tri-state data output lines (*Data* [0-9]) of several ATWD chips may be bussed together provided output enables (OE) is never applied to more than one chip at a time and enable to data propagation delays are observed.

Counter Reset must be pulsed before sample digitizing commences or after the data is read out. Failure to pulse *Counter Reset* will result in the counter counting forward from the currently registered counts when the next digitizing cycle is initiated.

One must assume that conversion may be complete before resources are available to read out the data.

When reading out the ATWD with a CPU, DSP or FPGA based readout engine, one might waiting in a loop until the ATWD is done converting, then reading digital data out. This strategy is satisfactory for a simple system with few data channels. Dead time may be high. Dead time may be reduced by pipelining or overlapping operations.

2. Absolute Maximum Ratings

Port	Absolute Maximum Range	Suggested operating point
Analog Supply Voltage	(V_{DD} to V_{SS}) +5.5V	+5.0 V
Digital Supply Voltage	+5.5V	+5.0 V
Analog Input Voltage input	[Analog Reference] to [V_{DD}+0.2]	0.3 to 3.5 V
Digital Input Voltage inputs	[V_{SS}-0.2] to [V_{DD}+0.2]	TTL or CMOS levels
Trigger Bias Current input	[V_{SS}-0.2] to [V_{DD}+0.2]	As required to set sample rate
Ramp Top Voltage input	[V_{SS}-0.2] to [V_{DD}+0.2]	3.15 V
Op-Amp Bias Current input	[V_{SS}-0.2] to [V_{DD}+0.2]	23 µA (100K pgm resistor)
Comparator Bias Current input	[V_{SS}-0.2] to [V_{DD}+0.2]	38 µA (100K pgm resistor)
Ramp Bias Current input	[V_{SS}-0.2] to [V_{DD}+0.2]	As required to set range
Analog Reference Voltage input	[V_{SS}-0.2] to [V_{DD}+0.2]	0.6 to 3.0 V
Comparator Bias Voltage input	[V_{SS}-0.2] to [V_{DD}+0.2]	0.6 to 3.0 V

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3. Electrical Characteristics

The limits stated above are largely speculative since insufficient resources were available to confirm damage limits. These limits are believed to be reasonable based on experience with other devices manufactured with the same process.

3.1 Pin Descriptions

Digital Signals	Function
Trigger	Initiate transient capture input
Trigger Complete	Goes low four sample rate periods before the last sampling aperture is closed.
Counter Clear	Pulse before digitizing or after readout to clear the ADC counters.
Counter Disable	When high, inhibits the Wilkinson counters. Must be low while digitizing and during the shifting out of digitized data.
Analog Reset	Clear any residual charge from charge sensing amplifier.
Read/$\overline{\text{Write}}$	Acquire/readout mode control. Low when capturing waveform, high when digitizing waveform.
Ramp Reset	When high, clamps ADC comparator input to Ramp Top Voltage. When low, the ramp current source causes the digitizer comparator input to sweep the ADC voltage range.
Counter Clock	The ADC counter increments one count per edge. Either edge may be first.

[3] Shannon Jackson at JPL chose to operate ATWR chips at V_{DD}=6V for performance reasons. One of two deployed devices eventually (apparently) failed. Since the failed device could not be recovered for postmortem, the reason for failure cannot be positively ascertained. Candidate failure modes are overvoltage, transient to an input, or latch-up related failure.

Shift Clock	Shifts data out of the ADC latch array. One datum per cycle. Data becomes 10 to 20 ns after the edge. Must be low while digitizing.
Output Enable	Tri-state digital data output enable input
Data [0--9]	Gray code encoded digitizer outputs. Data0 is the LSB.
Analog Controls	Function
Trigger Bias	Controls the sample capture rate. Higher current corresponds to faster sampling rate
Ramp Current Bias	Controls digitizer ramp rate. Program ramp rate with resistor to ground. Higher current corresponds to faster ADC ramp rate.
Ramp Top Voltage	Sets the ADC maximum comparator voltage. The ADC ramp voltage decreases linearly from this value when Ramp Reset goes Low.
Comparator Bias	Controls the operating point of comparator circuit.
Op-Amp Bias	Controls the operating point of input op-amp.
Analog Reference	Voltage applied to the lower end of waveform sample capacitors. Bypass with large value low inductance capacitor close to the chip.
Op-Amp Reference	Voltage applied to the inverting input of the ADC input op-amp.

3.2 Input and Output characteristics

3.2.1 Analog characteristics

Ramp top = 3.0, Analog Bias = 3.010

Parameter	symbol	conditions	min.	typ	max.	Units
Noise (RMS)		2.5V span		1		mV
Spatial noise (peak to peak)		Vin=1.75V		50		MV
Channel-to-Channel Crosstalk						mV

[4] Counter clock duty cycle **significantly** affects ADC differential nonlinearity. 50% duty cycle is nearly optimum.

[5] Higher bias current increases comparator bandwidth and reduces noise. Excessive bias current restricts the linear range of the stage. Lower bias current improves stage gain and linearity.

3.2.2 Typical operating Voltages and Currents

(V_{DD} = +5 V, V_{SS} = 0V)

Parameter	symbol	conditions	min.	typ	max.	Units
Analog Input Voltage		Vdd = 5.0 V		0.6	3.0	V
Digital Output Voltage High	V_{OH}	1 TTL Load	4.0	4.9		V
Digital Output Voltage Low	V_{OL}	1 TTL Load		0.2	0.5	V
Digital Input Voltage High	V_{IH}		2.45	2.95		V
Digital Input Voltage Low	V_{IL}			1.75	2.25	V
Digital Input Current High	I_{IH}	Vin = 4.5			<10	µA
Digital Input Current Low	I_{IL}	Vin = 0.0			<-10	µA
Analog Reference Voltage	V_{IR}		0.6	2.5	3.25	V†
Op-Amp Reference Voltage	V_{AR}		0.6	2.5	3.25	V†
Ramp Bias Current		20 µs ramp		157		µA
Ramp Top Voltage				3.15	3.5	V††
Comparator Bias Current		100K to Gnd		38		µA
Op-Amp Bias Current		100K to Gnd		23		µA
Trigger Bias Current		1 Gs/s		690		µA

† Above 3.25 V, at room temperature, the stage behavior changes abruptly. Operating the Analog Reference Voltage below the Analog Input Voltage results in diminished linearity.

††The Ramp Top Voltage should be operated approximately 10 mV or more negative than the Op-Amp Reference Voltage. Linearity near zero counts diminishes abruptly as Ramp Top Voltage nears Op-Amp Reference Voltage.

3.2.3 Fault Indications.

Substantial differences from the performance indicated below suggests that the die may be malfunctioning or demonstrating a manufacturing defect.

The Op-Amp Bias Current terminal is one leg of a current mirror. A short circuit from the Op-Amp Bias Current pin to ground will draw approximately 220 µA at room temperature.

The Comparator Bias Current terminal is one leg of a current mirror. A short circuit from the Comparator Bias Current pin to ground will draw approximately 3.5 mA at room temperature.

The Ramp Bias Current terminal is one leg of a current mirror. A short circuit from the Comparator Bias Current pin to ground will draw approximately 1.17 mA at room temperature.

The Capture Rate Bias Current terminal is one leg of a current mirror. A short circuit from the Comparator Bias Current pin **to Vdd** will draw approximately 7.3 mA at room temperature.

Data output line driver FET impedances less than 50 ohm or greater than 1000 ohm probably indicate a defective die. With a 1.25K ohm resistor form output to a 2.5V reference, 4.9V>Voh>3.9V, and 1.1V>Vol>0.2V.

3.3 Timing Characteristics (* indicates suggested value)

Parameter	symbol	Timing Reference	min	typ	max	Units
Read/Write Low to Trigger High Setup time		1 (4.1.2)	10 * [6]	?		ns
Trigger Complete Low to Trigger Low		2 (4.1.2)	10 * [7]		[8]	ns
Trigger Complete High to Trigger High Setup time		3 (4.1.3)	10 * [9]			ns
Channel Select to Analog Reset Low Settling Time		4 (4.1.4)	10 *	?		ns
Analog Reset Low to Read/Write High Setup Time		5 (4.1.4)	0 *	0	20 [10]	ns
Ramp Reset Low to Counter Disable Low		6 (4.1.4)		0 *		ns
Ramp Reset Low to Counter Clock edge Setup time (either edge)		7 (4.1.4)	10 *	20	LSB[11]	ns
Counter Disable Low to Counter Clock Edge Setup Time (either edge)		8 (4.1.4)	?	10 *		ns
Last Counter Clock Edge to Ramp Reset High Hold Time		9 (4.1.5)	0	>10		ns
Counter Clock Edge to Output Enable High		10 (4.1.5)	0	>10*		ns
Output Enable High to Data Valid propagation delay		11 (4.1.5)	15	20 *		ns
Ramp Reset Delay		12 (4.1.5)	1 (?)			µs
Shift Clock Low to Data Valid propagation delay		13 (4.1.5)	18	20 *		ns
Shift Clock Period		14 (4.1.5)	4	>8 *		ns
Data Hi/Low – Low/Hi Skew		(4.1.5)		2.5		ns
Data out Rise Time		(4.1.5)	2			ns
Data out Fall Time		(4.1.5)	2.5			ns
Shift Clock Low to Read/Write Low		15 (4.1.6)	0	10		ns
Read/Write Low to Analog Reset High Setup Time		16 (4.1.6)	5	10		ns
Mux and Buffer Settling Time		17 (4.1.7)	20	20 ??		ns
Output Enable Low to Data Invalid Propagation delay		18 (4.1.6)	15		18	ns
Post-Readout settling time		19 (4.1.6)	???	20		Ns

[6] 100 ns minimum settling time before next trigger preferable to insure low noise performance.

[7] 4 sample periods required for last sample aperture to closes.

[4] Trigger may be held high throughout the readout sequence without degradation

[9] 100 ns settling time is suggested to insure low noise performance.

[10] Minimize the float time of the op-amp. Measurements indicate signal loss associated with op-amp float.

[11] LSB corresponds to the half width of a digitizer clock full cycle. Time must be allowed for the ramp voltage to reach an equilibrium rate of change.

4. The Digital Interface

4.2 First suggested timing diagram.

Digitize/read-out logic simplicity, noise coupling and settling time issues drive the design of the read out engine which manipulates the ATWD. Appropriate delays must be introduced in the pattern to assure that conversion does not commence before the amplifiers have settled to within _ LSB.

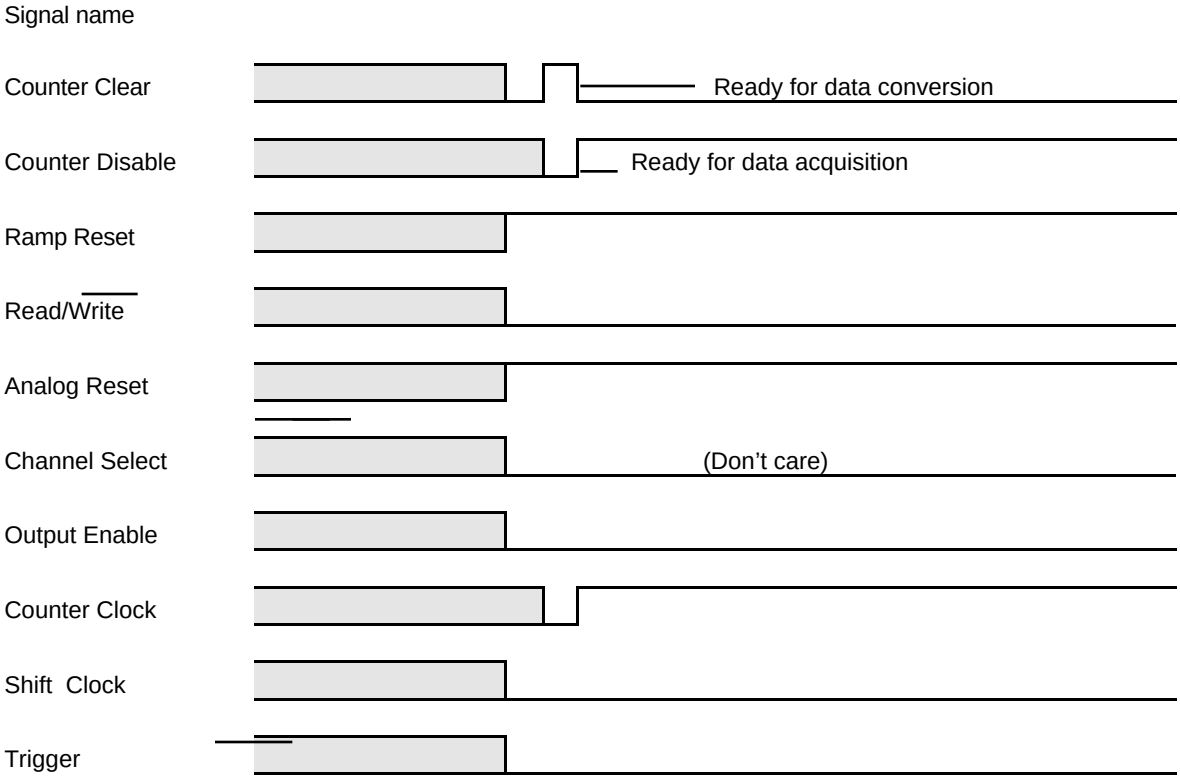
The suggested readout design further assumes that analog signals may be adversely affected by digital signals. Unnecessary digital transitions during signal acquisition and conversion are avoided.

In the interest of saving clock cycles, an attempt is made to overlap clock edges wherever possible as long as the data quality does not suffer.

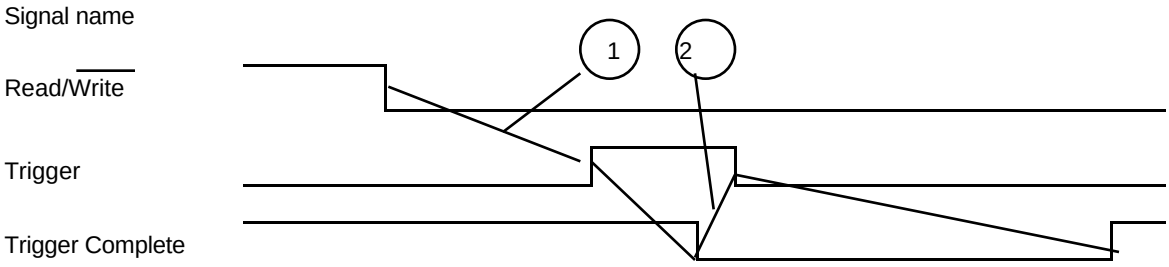
As you study the diagrams below you will find there is an ‘a’ path and a ‘b’ path. The important issue is whether one wishes to digitize, then move on to another channel, or to digitize, than digitize again, them move on.

For instance, one can digitize the first part of the dynamic range, and if justified, digitize the full dynamic range. One would first follow the ‘b’ path, then the ‘b’ path. One can switch tracks from the ‘b’ path to the ‘a’ path at the conclusion of digitizing.

4.2.1 Initializing for Data Taking

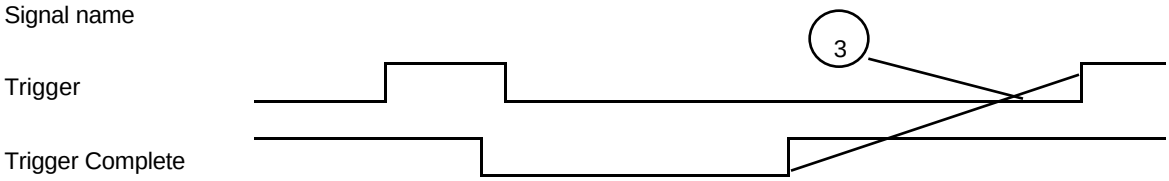


4.2.2 Transient Capture timing



	Recommended state	Optional state
Ramp Reset	High	-
Output Enable	Low	-
Analog Reset	High	-
Shift Clock	Low	-
Counter Clock	High	Stable high or low
Counter Disable	High	-
Counter Clear	Low	-
Channel select	Stable high or low	-

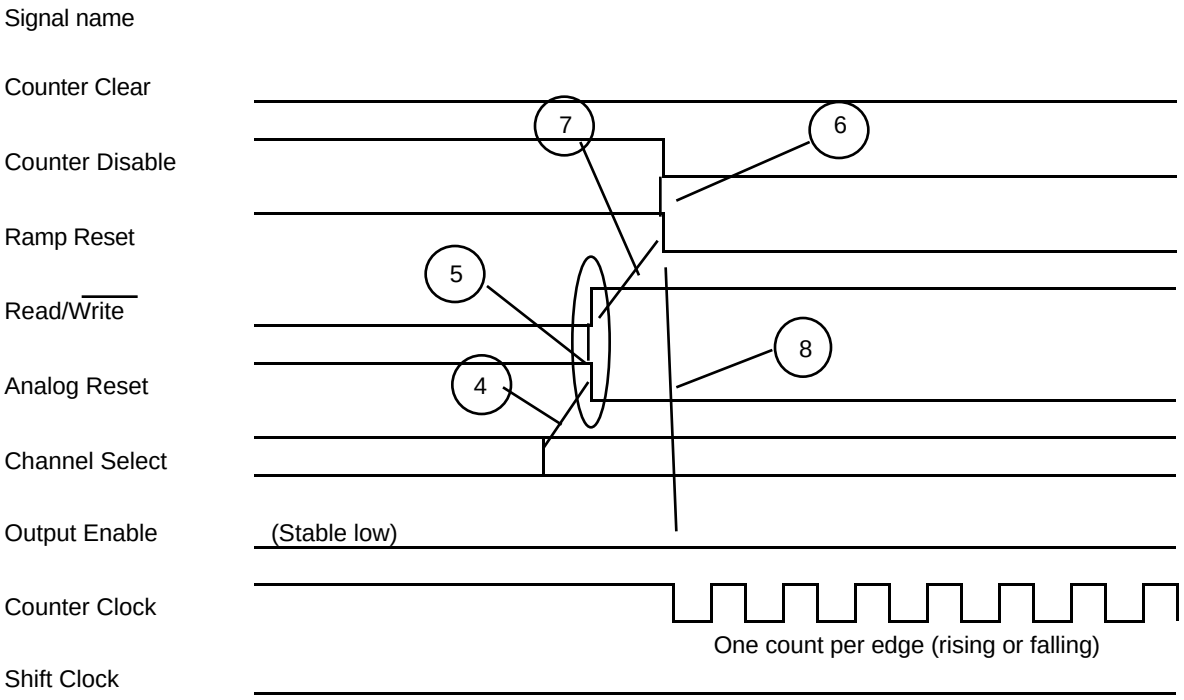
4.2.3 Timing for the case of an acquire event which is not followed by a digitizing cycle



	Recommended state	Optional state
Read/Write	Low	-
Ramp Reset	High	-
Output Enable	Low	-
Analog Reset	High	-
Shift Clock	High	Stable high or low
Counter Disable	High	-
Counter Clear	Low	-
Counter Clock	High	Stable high or low
Channel select	Stable high or low	-

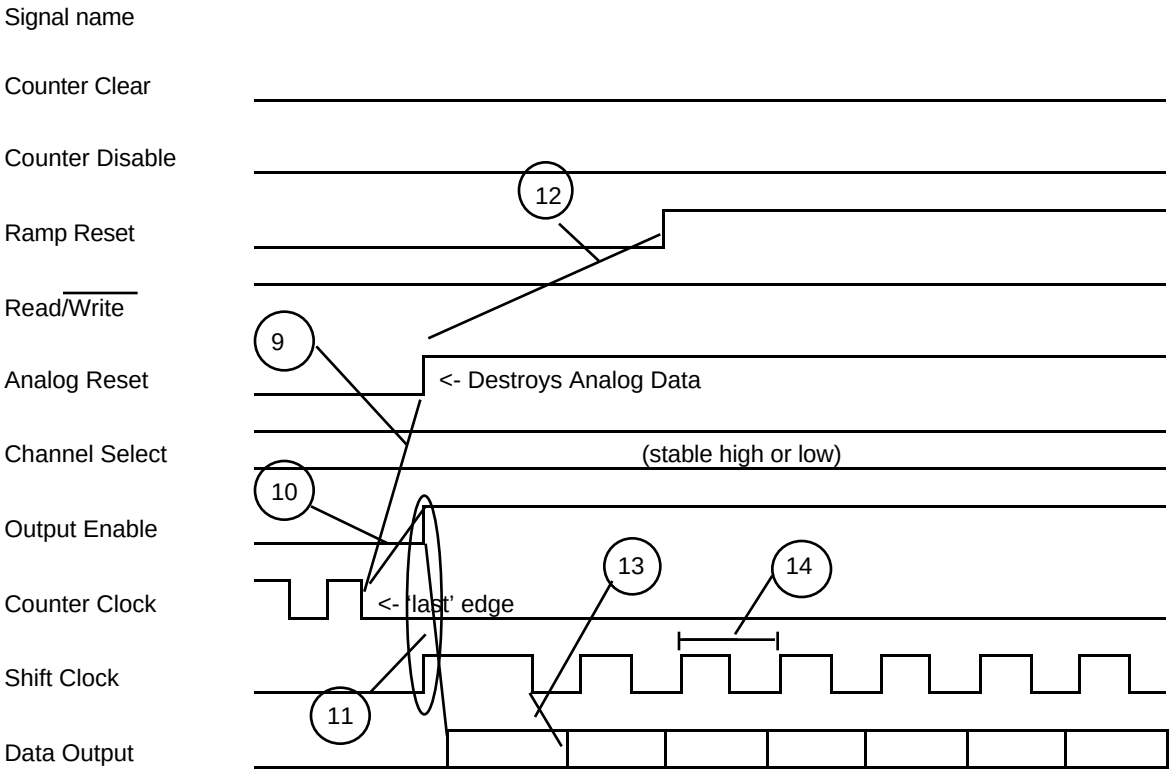
Acquired data need not be digitized before new data is acquired.

4.2.4 Transition from Acquire mode to Digitize mode timing (First channel to be read out)



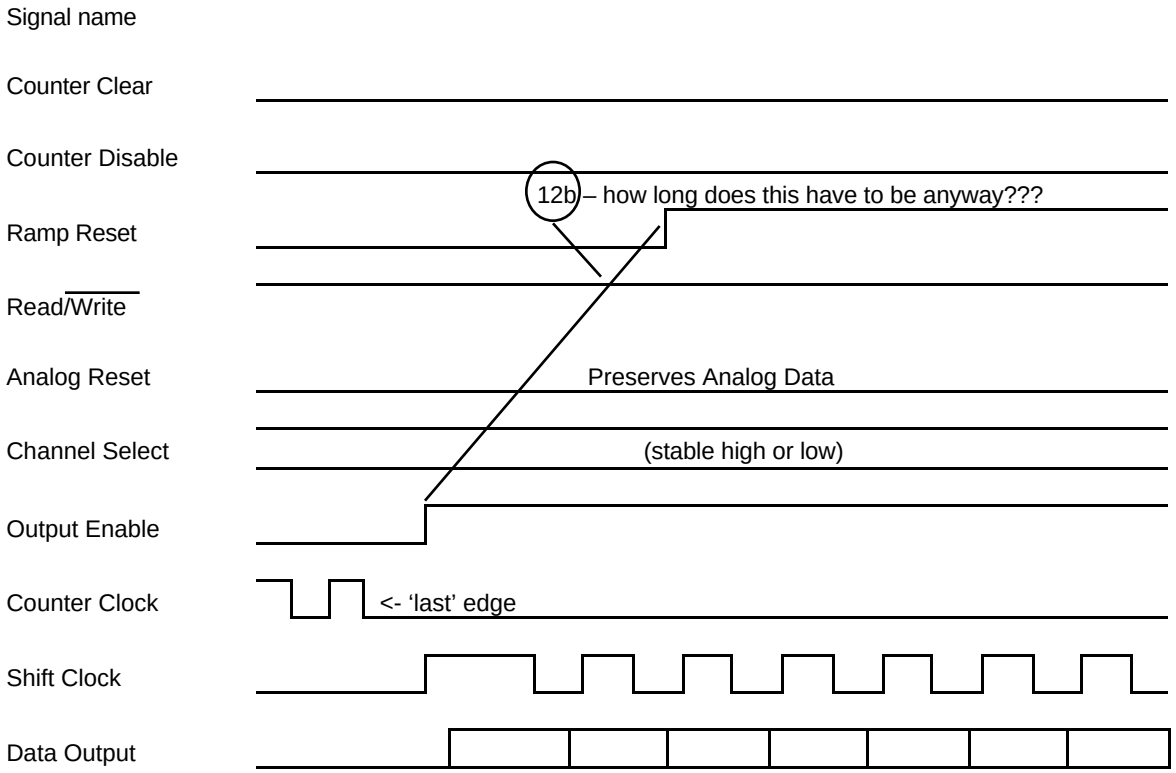
4.2.5a Transition from digitize mode to readout mode timing (First channel to be read out)

This example destroys the stored data immediately after conversion. Redigitizing is precluded.

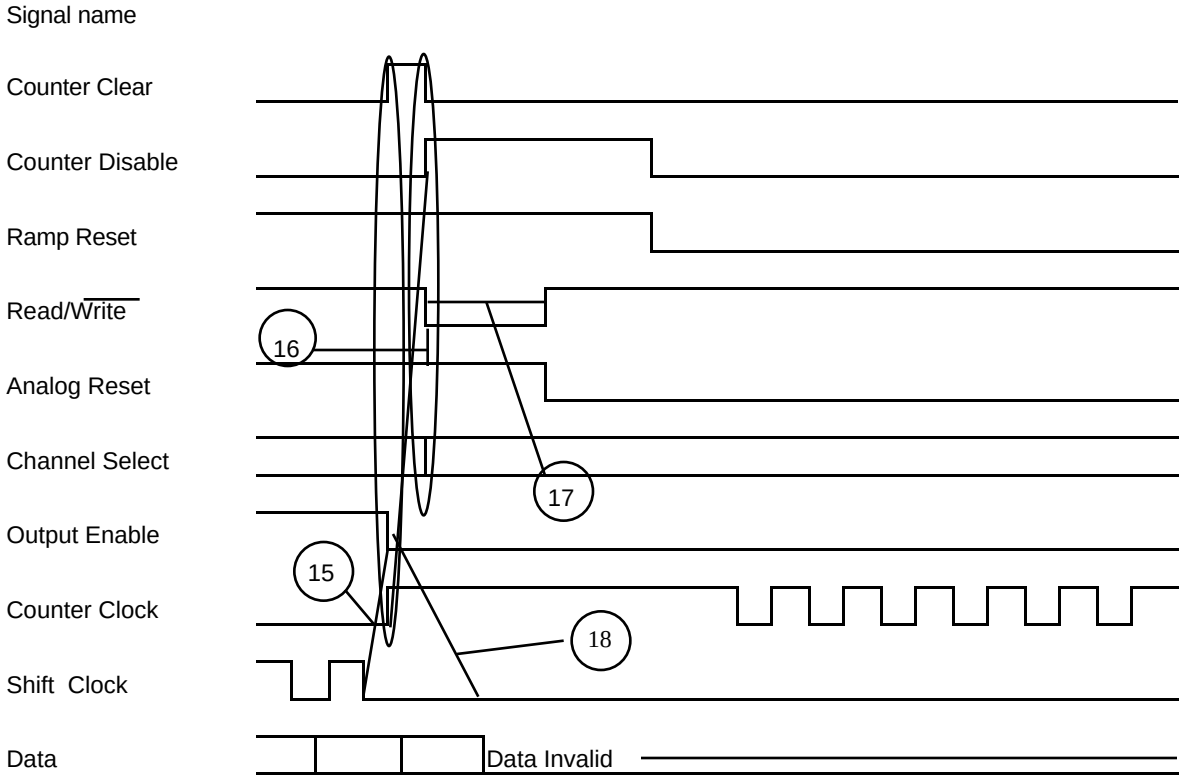


4.2.5b Transition from digitize mode to readout mode timing (First channel to be read out)

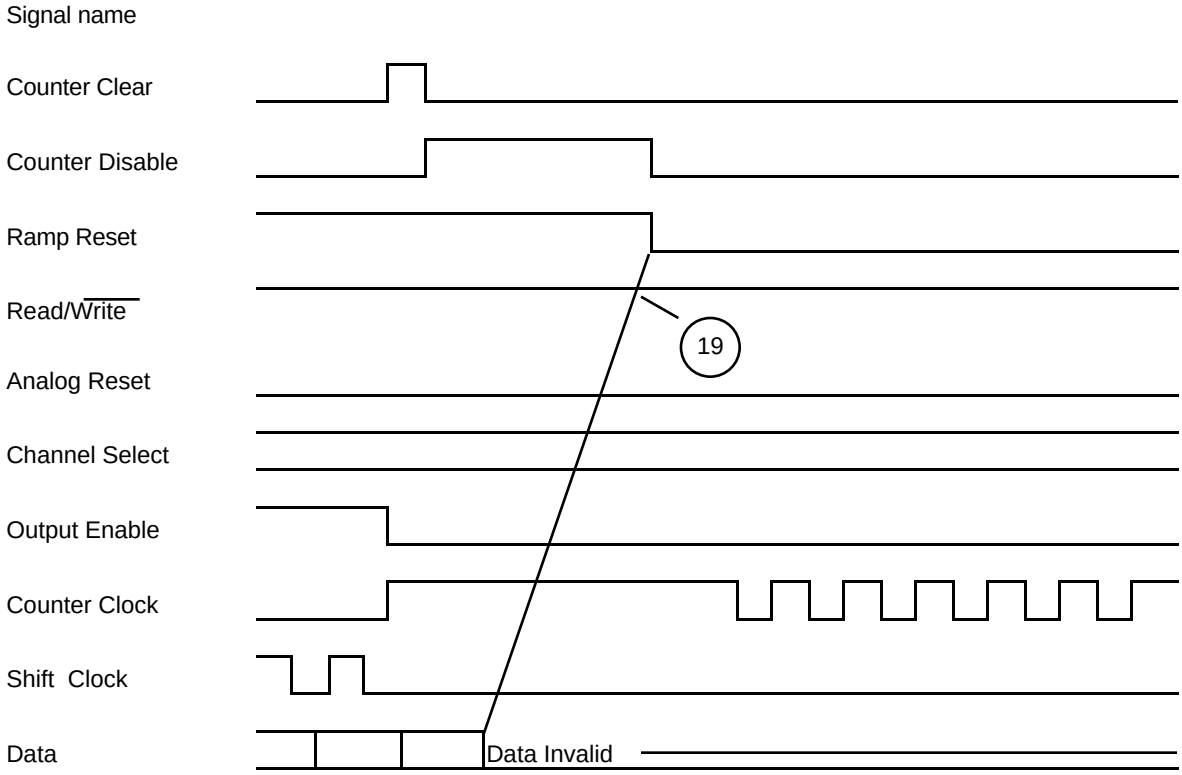
This example preserves the analog data. Redigitizing and readout is an available option.



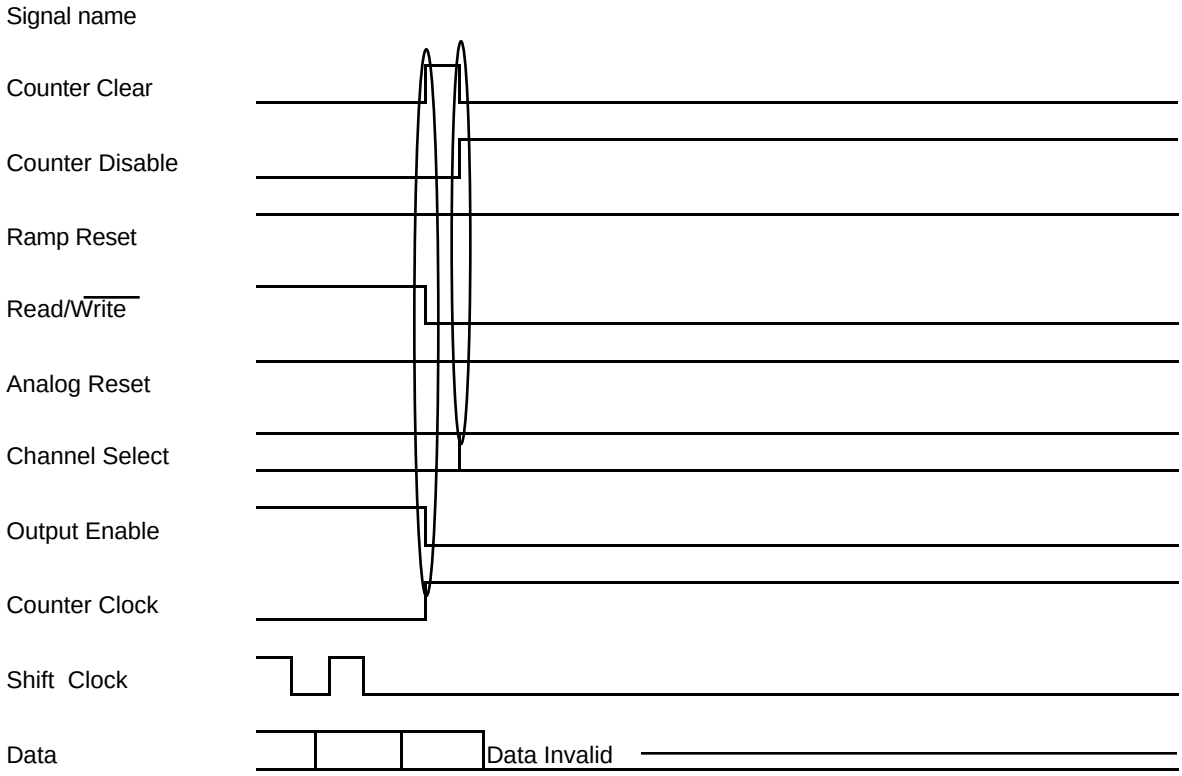
4.2.6a Transition from end of readout mode through change channel mode to begin digitize mode. Channel change is performed. Analog Data was destroyed. (Matches up with 4.2.5a)



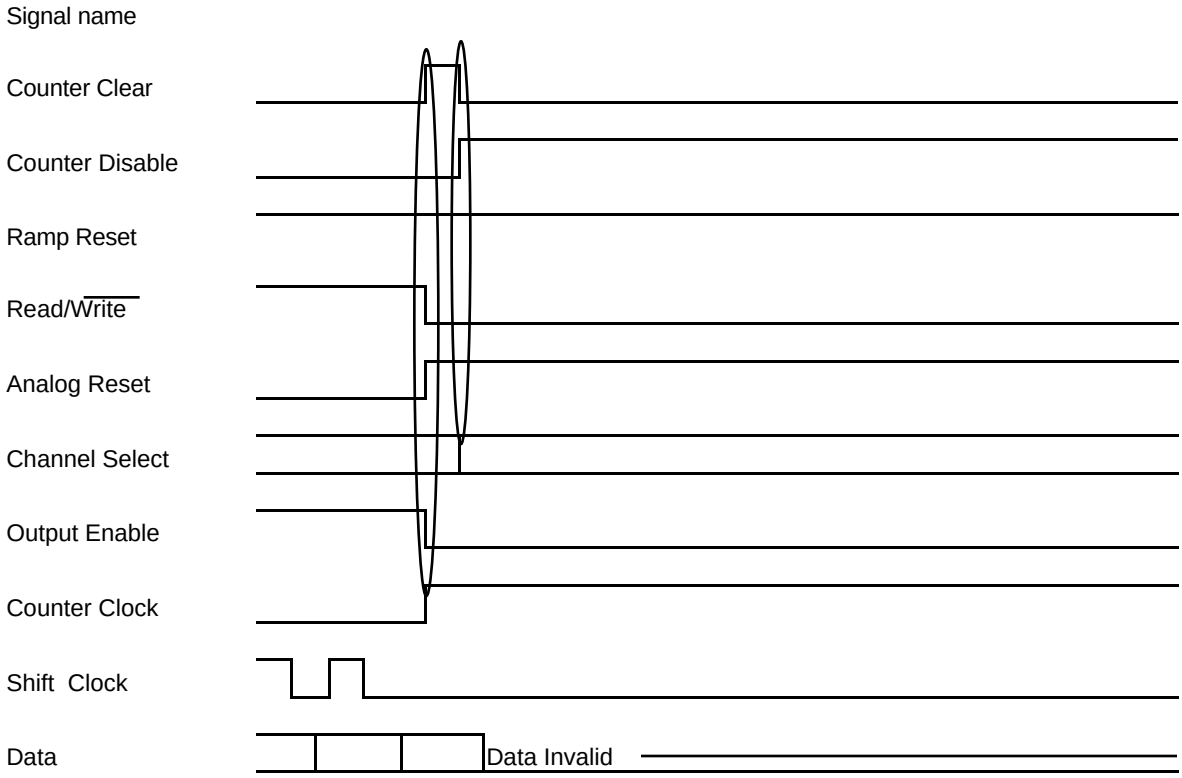
4.2.6b Transition from end of readout mode through change channel mode to begin digitize mode. Channel change NOT performed. Redigitizing initiated. . (Matches up with 4.2.5b)



4.2.7a Transition from end of readout mode to Acquire mode



4.2.7b Transition from end of readout mode to Acquire mode



5. PC Layout issues

As with all high-speed components, careful attention to layout is essential for best performance.

1) Use a printed circuit board with an unbroken ground plane.

2) Pay close attention to the bandwidth of bypass components. Place bypass capacitors close to the power pads of the chip or to the carrier contacts.

3) Bond all power and ground pads to carrier or PC board pads.

4) Keep lead lengths short to minimize inductances and stray capacitences. Parallel bonds to input and analog ground pads may enhance high frequency performance. Terminate close to the input pads.

6. Die Bonding

The die should be bonded and sealed in a carrier if the operating environment is humid or dirty. If possible, choose a chip carrier that will facilitate a design with short lead lengths. Dual in-line or flat pack carriers may be used provided the chip is oriented so that the die analog signal input pads bond out to pins with the shortest carrier leads. Quad carriers or pin-grid carriers are recommended to minimize lead lengths. When mounting the ATWD die in a carrier, the well in the carrier should be the smallest which will accommodate the die. When cementing the chip in the carrier, abut the input edge of the chip to the side of the carrier well. This will facilitate bonding out the pads with the shortest possible wires, a technique that will minimize lead inductance. Over sized signal input pads and reference pads allow the installation of multiple bond wires to further reduce inductance.

The substrate of the chip need not be grounded or bonded out to a pin. The substrate is not highly doped.

Chips may be mounted directly on circuit boards and bonded to circuit foils provided the bond wire is compatible with both the die pads and circuit foils. Gold flashed PC boards may be bonded to. The chip is passivated, so will not suffer if exposed to a benign environment. The application of a conformal coating to the die itself is not recommended since no compatibility or life testing of such a configuration of materials has been done. Chemicals in the conformal coating might attack the die, or the pad to wire bond.

7. State of the evolution

The Analog Transient Waveform Recorder chip design realized in1995 was built into hardware deployed at the South Pole in January 1997. Even as the first chips were characterized, the advantages of incorporating internal digitizers were noted. The first production ATWD dice fell just short of delivering the expected functionality. Nevertheless, the functionality was confirmed and some characterization was possible. As of this writing, the next version of the ATWD will be delivered in late April '98. Many parameters that are speculated upon in this document will be confirmed by testing.