July 22, 2000 GTP Change footprint for FPGA to one which has the pin names back annotated from the FPGA program design.

July 22, 2000 GTP Change Trigger Discriminator Signal names to match up to how the circuits are biased.

List of changes yet to be done:

On Local_Coincidence page, Explore the replacement of power splitters with transformers, but keeping in mind that isolation may suffer at high frequencies

Keep 1 inch x 1.75 inch space clear on top side of board for barcode label.

Power:	constant		transient
AD/DA page	31.5mW	+	65 mW
Analog Frontend	135 mW		
CPU	?		
PLD	?		
ATWD	120+2xATWD		
Communications	300 mW ??		
HS ADC	100 mW		
Local Coincidence	36 mW		
Memory	150mW		SDRAM
Memory	274.5mW		SRAM if accessed
Memory	?		Flash

CHECK PRINT 1/9/04

Title	IceCube - Digital Optical Module Main Board	
Size: B	Document Number: main_board_vsn4.1 sheet 1	Rev: 12.0
Date: Wednesday, October 09, 2002	Sheet 1 of 14	

Layer Stack-up

EVENSTAR BUILD UP AS OF 3/20/03
PLEASE NOTE: SHUFFLED STACKUP

1/2 OZ. TOP LAYER	ARTWORK 1
0.0036" PREPREG	
1/2 OZ. INNER TRACE LAYER	ARTWORK 2
0.004" LAMINATE	
1/2 OZ. INNER TRACE LAYER	ARTWORK 3
0.0036" PREPREG	
1 OZ. PLANE	ARTWORK 9
0.004" LAMINATE	
1 OZ. PLANE	ARTWORK 10
0.0036" PREPREG	
1 OZ. PLANE	ARTWORK 11
0.004" LAMINATE	
1 OZ. PLANE	ARTWORK 13
0.0036" PREPREG	
1 OZ. PLANE	ARTWORK 9
0.004" LAMINATE	
1 OZ. PLANE	ARTWORK 12
0.0036" PREPREG	
1 OZ. PLANE	ARTWORK 14
0.004" LAMINATE	
1 OZ. PLANE	ARTWORK 9
0.0036" PREPREG	
1/2 OZ. INNER TRACE LAYER	ARTWORK 4
0.004" LAMINATE	
1/2 OZ. INNER TRACE LAYER	ARTWORK 5
0.0036" PREPREG	
1/2 OZ. BOTTOM LAYER	ARTWORK 8

6 LAMINATES @ .004	= .024
7 PREPREG @ .0036	= .0252
11 OZ. COPPER @ .0014	= .0154
2 SOLDERMASK @ .0007	= .0015
FINAL BOARD THICKNESS	= .0661

CHECK PRINT 1/9/04

Title: IceCube - Digital Optical Module Main Board		
Size: B	Document Number: main_board_vsn4.1 sheet 2	Rev: 12.0
Date: Wednesday, October 09, 2002	Sheet 2 of 14	

If inductors L12 & L13 shift as the temp. decreases, it is possible to compensate by giving the capacitor the correct temp. coefficient.

5Vanalog

C392 100nF OPTIONAL

C394 100nF*

U64 MAX6126AASA

NR IC1 IN OUTF GND OUTS GNDS IC2

JU14 Open Ckt

JU15 Open Ckt

If U64 (MAX6126) is loaded then do not load R447

R447 20* 3.3V

C396 100nF

C404 100nF*

VCC OUT GND

Y2 20 MHz Toyocom Oscillator*

Fo

B50 EMI 0805-120*

C434 100nF*

L12 & L13 must not be parallel or end to end

T-Section Filter/ Impedance Matching

C453 100nF

TP38 2-Pin Header

R472 210*

R477 210*

L14 3.9uH@20MHz Delevan 1330-34K

L13 3.9uH@20MHz Delevan 1330-34K

TOYOCOM_OSC

C423 22pF NPO*

C426 10pF NPO*

U73 AD8005RT*

C447 30pF NPO including strays@20MHz

R496 100 1%

C445 100nF

C438 100nF*

R484 4.7K*

R483 4.7K*

R492 1K 3.3V

R488 Open Ckt Bias adjustment

R470 200 Amplitude adjustment

R464 20*

C408 100nF*

3.3V R436 10K 1%*

R442 10K 1%*

R455 10K 1%*

R451 10K 1%*

C398 100nF*

Latch

U68 MAX9013EUA*

R461 2.7K*

3.3V C400 100nF

U71 DS90LV017ATM

CLK nCLK

R468 4.7K*

C379 100nF

Y1 CORNING_2560

Vdd NC OUT GND1 GND2

Square wave output

Corning Frequency Control Model C2560A-0009

* = DNL

CHECK PRINT 1/9/04

rev 11/18/02 rhm/ GTP			
Title: Digital Optical Module Crystal			
Size: B	Document Number: main_board_vsn4.1 sheet 3 of 14		Rev: 12.0
Date: Wednesday, October 09, 2002	Sheet 14 of 14		

4

Over-Voltage protection for the power supply. I suppose, this could as easily be balanced, using just the N and P FETs. If it is deemed that the power supply input voltage range(and tolerance) is great enough, the protection circuit can be deleted from the design.

NOVAcap1812Z474M25INX250V
Z5U Ceramic Capacitor

L12
Digi-Key Panasonic
PK1064-ND ELF-15N002A

DCIN1
DCIN2
C159 470nF 250V
B28 EMI 1812-125
B29 EMI 1812-125

JP13
HEADER_4X2*

For development: A daughter card plugged into JP15 can be used to design an appropriate filter network.

CR20 CMHZ5263B*
CR19 CMHZ5263B*
CR21 CMHZ5235B*
CR22 CMHZ5235B*
R146 10K 1%*
R154 10K 1%*
R134 10M*
Q6 2N7002*
Q2 IRF644NS* D2PAK

JU3 Jumper
C133 470nF 250V

L10 Delevan SPD73-334
L11 Delevan SPD73-334
LAYOUT TO AVOID MAGNETIC COUPLING

90V_Neg
90V_Pos

C110 10uF 16V
B24 Delevan SMB2.5-1
B25 Delevan SMB2.5-1
C131 470nF 250V
C142 470nF 250V
DEARBORN 730P106X9160
ADD GND PAD FOR SHIELDING

PS2
70 IMX 4-05-05-9
Power-One
Vin+ Vin+ +5V COM Vin- Vin- -5V
40-120V

DUAL FOOTPRINT OPTION TO LOAD PS1 OR PS2

PS1
70 IMX 7-05-05-9
Power-One
Vin+ NC Vo2+ Vo2- Vo1+ Vo1- Trim Vin- Inh
40-120V

+5V_unfiltered
-5V_unfiltered
-5V_supply

WIDE TRACES
WIDE TRACES

R68 0.100
R88 0.100
+5V
-5V

B11 EMI 1812-125
B14 EMI 1812-125
B18 EMI 1812-125
B16 EMI 1812-125

C97 100nF
C90 100nF
C108 100nF
C123 100nF
C124 100nF
C109 100nF

5Vanalog
C93 47uF-6.3V Tan EEU-FC1E470P10267-ND
C103 47uF-6.3V Tan EEU-FC1E470P10267-ND

CR11 BAV103-7
CR12 BAV103-7
CR9 BAV103-7
CR8 BAV103-7
-3.3V
6.6Vanalog
C122 2.2uF 16V Tan
C116 2.2uF 16V Tan
C121 2.2uF 16V Tan
C104 2.2uF 16V Tan

U8
MAX1702BEGX
INP1 LX1 OUT1 INP2 COMP1 INP3 Vdd DBI LBI LX2 FB2 COMP2 LX3 OUT3 COMP3 -LBO -RSO OUTOK ON2 -MR PGM3 REF GND GND PGD2 PGD1

R53 0.100
+3.3V_IN
C82 100nF
C79 OSCON_6SEP82M

R48 0.100
+2.5V_IN
C62 100nF
C66 OSCON_6SEP82M

R40 0.100
+1.8V_IN
C50 100nF
C46 OSCON_6SEP82M

+5V_unfiltered
C94 OSCON_6SEP82M
R51 316K
R50 30K
R46 100K 1%

OUT1
R37 Jumper
R49 Open Ckt
R56 10K 1%
R38 Open Ckt
nPOR
nURESET
Alternate power down-reset option.

L8 Delevan SPD62-402
L9 Delevan SPD62-103
B13 SMB2.5-1
C76 100nF
C102 OSCON_6SEP82M
C99 100nF
C106 100nF
C105 47uF-6.3V Tan
C95 100nF
3.3V

R55 30K
C71 33pF NPO
C80 3.3nF NPO
Switching inductor could possibly be 4.7uH. Need at least 1.5 A max current. Note that permeability decreases at low temperature.

L7 Delevan SPD62-402
L6 Delevan SPD62-103
B7 EMI 1812-125
R39 36.5K 1%
R32 14.0K 1%
C63 100nF
C67 OSCON_6SEP82M
C51 100nF
C77 100nF
C68 47uF-6.3V Tan
C78 100nF
C86 100nF
2.5V

R57 30K
C74 33pF NPO
C89 10nF NPO

L5 Delevan SPD62-402
L3 Delevan SPD62-103
B6 SMB2.5-1
C21 100nF
C23 OSCON_6SEP82M
C18 100nF
C25 100nF
C30 47uF-6.3V Tan
C19 100nF
C36 100nF
1.8V

R47 30K
C57 33pF NPO
C56 8nF NPO

Distribute widely around the PC board to improve noise suppression. If noise performance is good enough, some of these parts may be deleted from the final design. The design might benefit by additional bypassing on 3.3V.

The MAX1702 contains voltage monitoring circuitry, and staged start circuitry

C58 100nF

5Vanalog
-5V
C92 OSCON_6SEP82M
C185 OSCON_6SEP82M
C212 OSCON_6SEP82M
C112 OSCON_6SEP82M
C407 OSCON_6SEP82M
C96 100nF
C183 100nF
C225 100nF
C114 100nF
C413 100nF
C385 100nF
C184 100nF
C424 100nF
C12 100nF
C52 100nF
C377 OSCON_6SEP82M
C443 OSCON_6SEP82M
C414 OSCON_6SEP82M
C10 OSCON_6SEP82M
C22 OSCON_6SEP82M

U9 AD626AR
-5V_unfiltered
-5V_supply
C54 100nF
C65 100nF
Imon-5V
Assuming a 500 mW load on -5V, a gain of 100 yields a 1V signal to the ADC input.

U12 AD626AR
+5V_unfiltered
+5V
C70 100nF
Imon+5V
Assuming a 200 mW load on +5V, a gain of 100 yields a 400mV signal to the ADC input

U5 AD626AR
JU2 Jumper_Open Ckt
+5V_unfiltered
+3.3V_IN
C47 100nF
Imon+3.3V
Assuming a 500 mW load on +3.3V, a gain of 100 yields a 1V signal to the ADC input

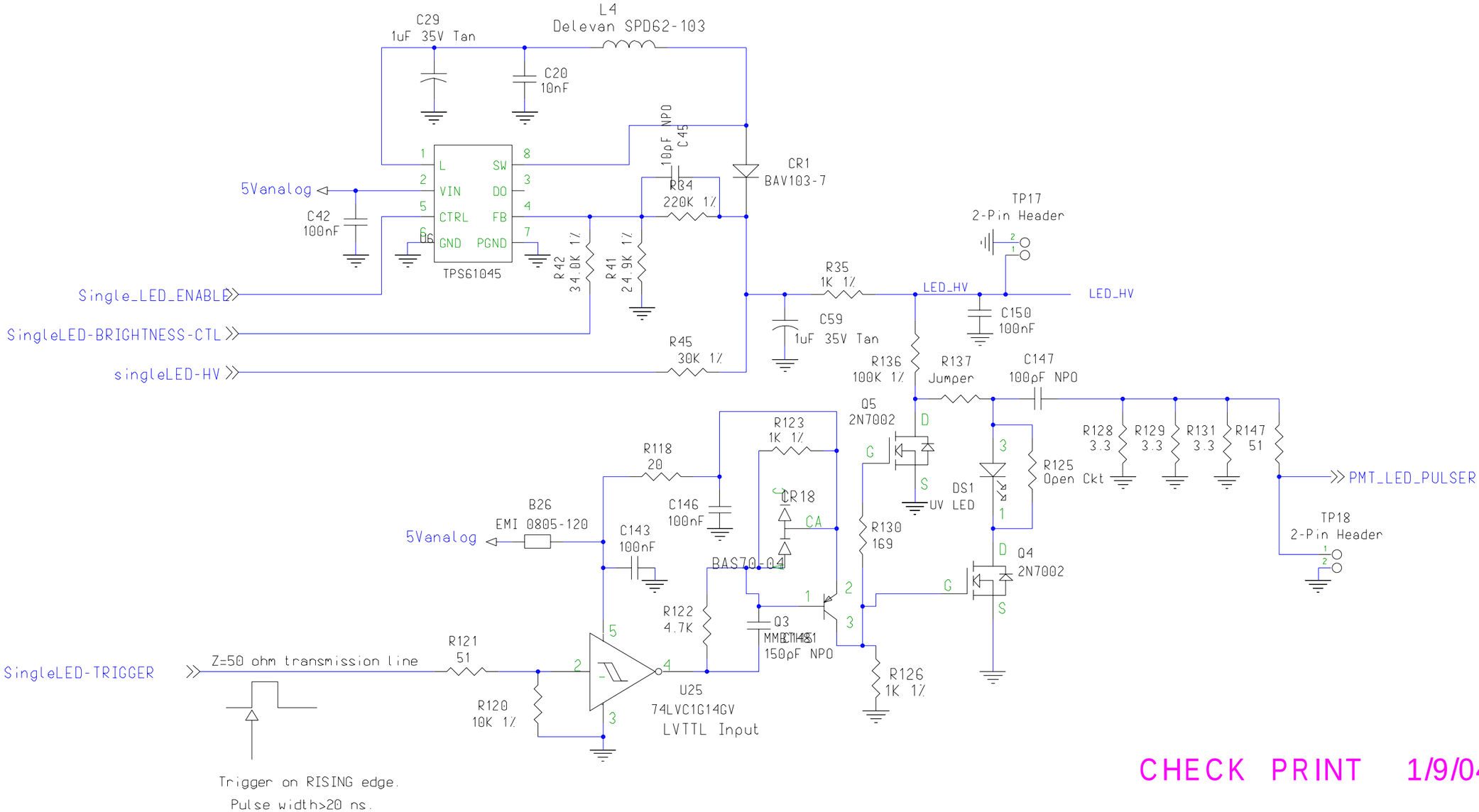
U7 AD626AR
+5V_unfiltered
+2.5V_IN
C41 100nF
Imon+2.5V
Assuming a 200 mW load on +2.5V, a gain of 100 yields a 400mV signal to the ADC input

U3 AD626AR
+5V_unfiltered
JU1 Jumper_Open Ckt
+1.8V_IN
C24 100nF
Imon+1.8V
Assuming a one Watt load on +1.8V, a gain of 10 yields a 200mV signal to the ADC input

CHECK PRINT 1/9/04

* = DNL

rev 11/19/02 rhm/gtp	rev 12/11/02 rhm repaired gnd symbol		
Title: Digital Optical Module Power Supply			
Size: C	Document Number: main_board_vsn4.1	sheet 4	Rev: 12.0
Date: Wednesday, October 09, 2002	Sheet 13 of 14		



CHECK PRINT 1/9/04

* = DNL

Title	Digital Optical Module Single LED		
Size B	Document Number main_board_vsn4.1 sheet 5		Rev 12.0
Date: Wednesday, October 09, 2002	Sheet 12 of 14		

Require MUX_EN4 low at power up
Require HV power supply control at power up, and through reloading the FPGA
BOOT_FLASH line control

Desmear
ADC and DAC control not depending on FPGA load (avoid glitches)
remember source of power failure
Flash Memory CSR remapping

DOM SERVICE MODE

An address space of 16 registers

U34
XC2C384_TQ144

BASE_MISO
CONF_DONE
SC_nCS2
OSR_Local
R184 100 1/
R191 100 1/
SC_nCS6
MUX_ENB
A_nB
SC_MISO
SC_nCS1
MUX_EN
SC_SCLK
SEL_A1
SOFT_RESET
nPOR
EX_TXD R344 100
EB00
EB01
EB02
EB03
EB04
EB05
EB06
EB07
INIT_DONE
EX_OSR
EX_CTS
nRESET
nSTATUS
SC_nCS0
EB_CLK
SC_nCS4
EB40
EB41
EB42
EB43
EB44
EB45
EB_nOE
EB_nWE
EB_nCS3
EB_nCS2
EB_nCS1
EB_nCS0
BOOT_FLASH
nCONFIG
INT_EXT_PIN_N
R258 10K 1/
R259 10K 1/
R241 10K 1/
PLD_FPGA_nWE
PLD_FPGA_nOE
PLD_FPGA_BUSY
PLD_FPGA_(0)
PLD_FPGA_(1)
PLD_FPGA_(2)
PLD_FPGA_(3)
PLD_FPGA_(4)
PLD_FPGA_(5)
PLD_FPGA_(6)
PLD_FPGA_(7)
R238 10K 1/
R239 10K 1/
R240 10K 1/
R179 10K 1/
PLD_TDI
PLD_TMS
PLD_TCK
PLD_TDO
BAROMETER_ENA
SC_MOSI
SEL_A0
FL_D0
FL_D1
FL_D2
FL_D3
FL_D4
FL_D5
FL_D6
FL_D7
SC_CL
FL_A0
FL_A1
FL_A2
FL_A3
FL_A4
FL_A5
R175 100 1/ CTS_Local
FL_nOE
FL_nWE
FL_ON_OFF
FL_JTAGEN
TXD_Local
R176 100 1/
R177 100 1/
AUX_CTL
SC_nCS5
SC_nCS3
R178 100 1/ RXD_Local
R185 100 1/
SC_nCS7
BASE_SCLK
BASE_ON-OFF
BASE_nCS1
BASE_nCS0
BASE_MOSI
EX_RXD
SER_PWR
DTR_Local
RTS_Local
R189 100 1/ EX_DTR
R196 100 1/ EX_RTS
EB_nPOR
BASE_HV_DISABLE
Single_LED_ENABLE
R205 10K 1/
R211 10K 1/
COMM_RESET
FLASH_nWP
FLASH_nWE
FLASH_nOE
FLASH_nCS1
FLASH_nCS0
FPGA_LOADED
R412 10K 1/
C169 10nF
C237 100nF
C188 100nF
C190 100nF
C208 100nF
C172 100nF
C160 10nF
C164 OSCON_6SEP82M
C175 100nF
C238 100nF
C182 100nF
C161 10nF
1.8V
3.3V
Require MUX_EN4 low at power up

R200 10K 1/
TP21
2 Pin Header
PLD_TP

R193 10K 1/
JP15
2 Pin Header

C189 100nF
R26 DS90LV018ATM
CLK
nCLK
R212 20
DS90LV018ATM

R187 4.7K
CR24 BAV103-7
TP22
2-Pin Header
S2
B3FS-1002P (Omron)
R194 Jumper
C192 100nF
Soft_RESET

R36 4.7K
CR2 BAV103-7
TP8
2-Pin Header
S1
B3FS-1002P (Omron)
R44 10K 1/
nURESET
5Vanalog
C53 47uF-6.3V Tant

EB07
EB06
EB05
EB04
EB03
EB02
EB01
EB00
EB[0:15]
EBA0
EBA1
EBA2
EBA3
EBA4
EBA5
EBA[0:24]

U50
EXCALIBUR_XA1G
IO_Bank_B7
EX_CTS
EX_DSR
EX_RXD
EX_TXD
EX_RTS
EX_DTR
UART_CTS_N
UART_DSR_N
UART_RXD
UART_DCD_N
UART_RI_N
UART_TXD
UART_RTS_N
UART_DTR_N
EPXA1F6721Z

R188 4.7K
R186 4.7K
Base_nCS0
Base_nCS1

JP11
RJ45 AMP 555764-1
DTE
CTS_in
DSR_in
CPU_SERIN1_RS232
CPU_SEROUT1_RS232
DTR_out
RTS_out
Per Lantronix Server documentation
Wired as DTEuse 1:1 cable toMODEM
Digi-Key A9045-ND

U24
MAX3241CWI
RTS_Local
TXD_Local
DTR_Local
RXD_Local
DSR_Local
CTS_Local
C139 100nF
C138 100nF
C127 100nF
C140 100nF
C141 100nF
-EN
-SHDN
VCC
CR17 BAV103-7
JP12
2 Pin Header
SER_PWR
R102 1K 1/
R103 10K 1/

DS4
BR1111C-TR4
R516 130*
EX_TXD
DS3
R515 130*
EX_RXD
DS2
R514 1K 1/*
INIT_DONE
R519 10K 1/
* = DNL

EPCBYPASS
EPCINLINE
JP10
0 100 2x2 SMD_HEADER
JTAG ROUTING
TDO
EPCTDO
TDO2TDI
EPCTDI
TMS
TCK
TDI

U50
EXCALIBUR_XA1I
Excalibur JTAG Ports
PROG_TMS
PROC_TDO
PROC_TDI
PROC_TCK
PROC_TRST
TRST
TDO
TMS
TCK
TDI
EPXA1F6721Z
R324 R325 R326 R327 R328 R329 R330 R331 R332
10K 1/

For bypassing the EPC2, jumper center to bridging position, pin 1 to pin 2
To put EPC2 into circuit, jumper pin1 to pin3, and pin2 to pin 4

U29
EPC2*
R134 R135
R132 R169 R165 R133
10K 1/
Vcc
VppSel
Vpp
VccSel
TCK
TMS
TDI
TDO
EPCTDO
nSTATUS
nCONFIG
DATA0
OCLK
CONF_DONE
nCS
nCASC
nINIT_CONF
DATA
GND
JU5
Open Ckt
TDO2TDI
JU4
Open Ckt
TDO
If it is found that the configuration is correct, JU11, and JU12 can be installed during manufacture

JP6
CPLD
BLACK
PLACE CPLD AND CPU CONNECTORS AT THE EDGE OF BOARD
CPU
GRAY
AMP 2510-6002UB_BLK
PLD_TCK
PLD_TDO
PLD_TMS
PLD_TDI
JP8
AMP 2510-6002UB
TCK
TDO
TMS
TDI
JP7
AMP 2510-6002UB*
PROC_TCK
PROC_TDO
PROC_TMS
PROC_TDI

U41
DS90LV017ATM
CLK*2
nCLK*2
C216 100nF
U63
DS90LV018ATM
CLK
nCLK
R417 20
TP35
2-Pin Header
C278 100nF
C391 100nF
INIT_DONE
TP23
2-Pin Header
Gnd
U61
74LVC1G125GV
OE
In
Out
R416 20
R413 1K 1/
CLKLK_ENA
PGM12
CLKLK_FB2p
CLKLK_FB2n
CLKLK_OUT2p
CLKLK_OUT2n
CLKIn
NC
R307 10K 1/
JU10
Open Ckt
JU11
Jumper
R325 10K 1/
R369 10K 1/
JU12
Open Ckt
nSTATUS
nCONFIG
DCLK
CONF_DONE
INIT_DONE
nRESET
EB_nPOR
BOOT_FLASH
Debug_nWatchdog
MSEL0
MSEL1
nCEO
nCE
nSTATUS
nCONFIG
DCLK
CONFIG_DONE
IO-INIT_DONE
JSELECT
EN_SELECT
nRESET
nPOR
BOOT_FLASH
DEBUG_EN
GND-*STDCEL_TEST
CS-IO
nCS-IO
nWS-IO
nRS-IO
RDYnBSY-IO
CLKUSR-IO
FAST_IO1
FAST_IO2
FAST_IO3
FAST_IO4
OneSPE
MultiSPE
IO-DATA7
IO-DATA6
IO-DATA5
IO-DATA4
IO-DATA3
IO-DATA2
IO-DATA1
DATA0
R264 Jumper
IO-DEV_CLRn
IO-DEV_OE
CLK_REF
CLK1p
IO-CLK1n
CLK2p
IO-CLK2n
CLK3p
IO-CLK3n
CLK4p
IO-CLK4n
LOCK1-IO
LOCK2-IO
LOCK3-IO
LOCK4-IO
PGM7
PGM8
PGM9
PGM10
GlobalClockInputs
EPXA1F6721Z
U50
EXCALIBUR_XA1J

C336 47pF NPO
R322 100 1/
OneSPE
OneSPE-C
C313 47pF NPO
R304 100 1/
MultiSPE
MultiSPE-C

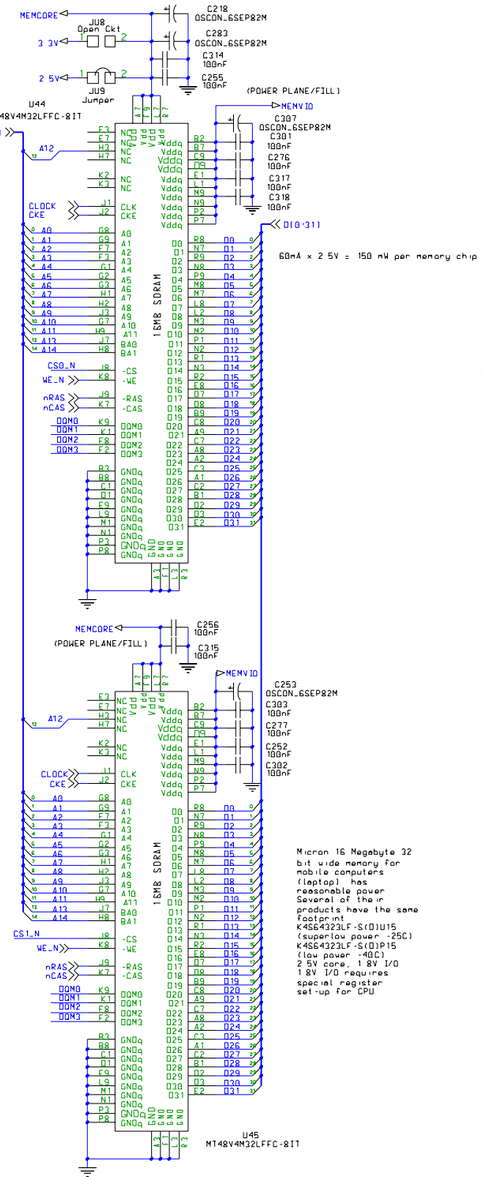
nCE = pull-down
nCEO = open ckt
TRST = pull-up
TDI = pull-up
TDO = pull-up
TMS = pull-up
TCK = pull-up
nSTATUS = pull-up
CONFIG_DONE = pull-up
nCONFIG = pull-up

JP20
2mm pitch SMD_HEADER_10X2*
PGM0
PGM1
PGM2
PGM3
PGM4
PGM5
PGM6
PGM7
PGM8
PGM9
PGM10
PGM11
PGM12
PGM13
PGM14
PGM15
Service Connector for the convenience of software programmers
Utilizes multifunction pins

U27
EPC4QI100
R119 1K 1/
C149 100nF
C148 100nF
BYTE#
PORSEL
WP#
TMOI
TMOO
nCS
OE
OE#
C-RP#
F-RP#
C-WE#
F-WE#
CE#
EXTCLK
A20*Float
A19*Float
A18
A17
F-A16
F-A15
A14
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
F-A1
F-A0
TDI
TDO
TMS
TCK
PGM2
PGM1
PGM0
nINIT_CONF
DCLK
-RY-BY#
DATA7
DATA6
DATA5
DATA4
DATA3
DATA2
DATA1
DATA0
DQ15
DQ14
DQ13
DQ12
DQ11
DQ10
DQ9
DQ8
DQ7
DQ6
DQ5
DQ4
DQ3
DQ2
DQ1
DQ0
C-A16
C-A15
C-A1
C-A0
Float
nCONFIG
DCLK
DATA0

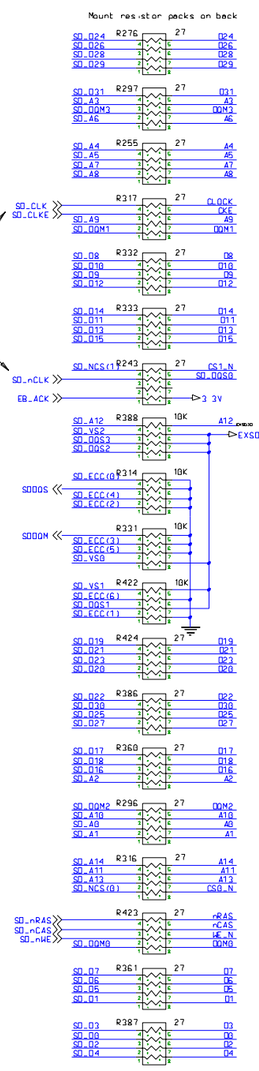
CHECK PRINT 1/9/04

rev 11/18/02 rhn, GTP	
Title	Digital Optical Module CPU
Size: D	Document Number: main_board_vsn4 1 sheet 6
Rev: 12 B	
Date: Wednesday, October 09, 2002	Sheet 11 of 14

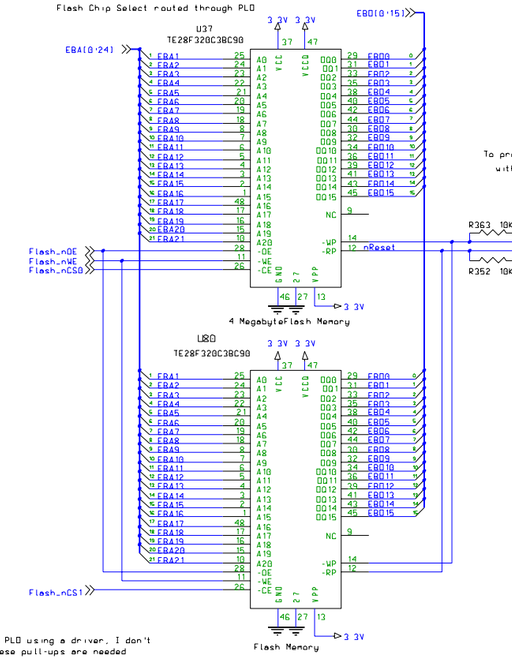


Mount resistor packs on back

SD_nCLK must make a loop of approx same length as SD_CLK to match timing
See HW Ref Manual



Flash Chip Select routed through PLD

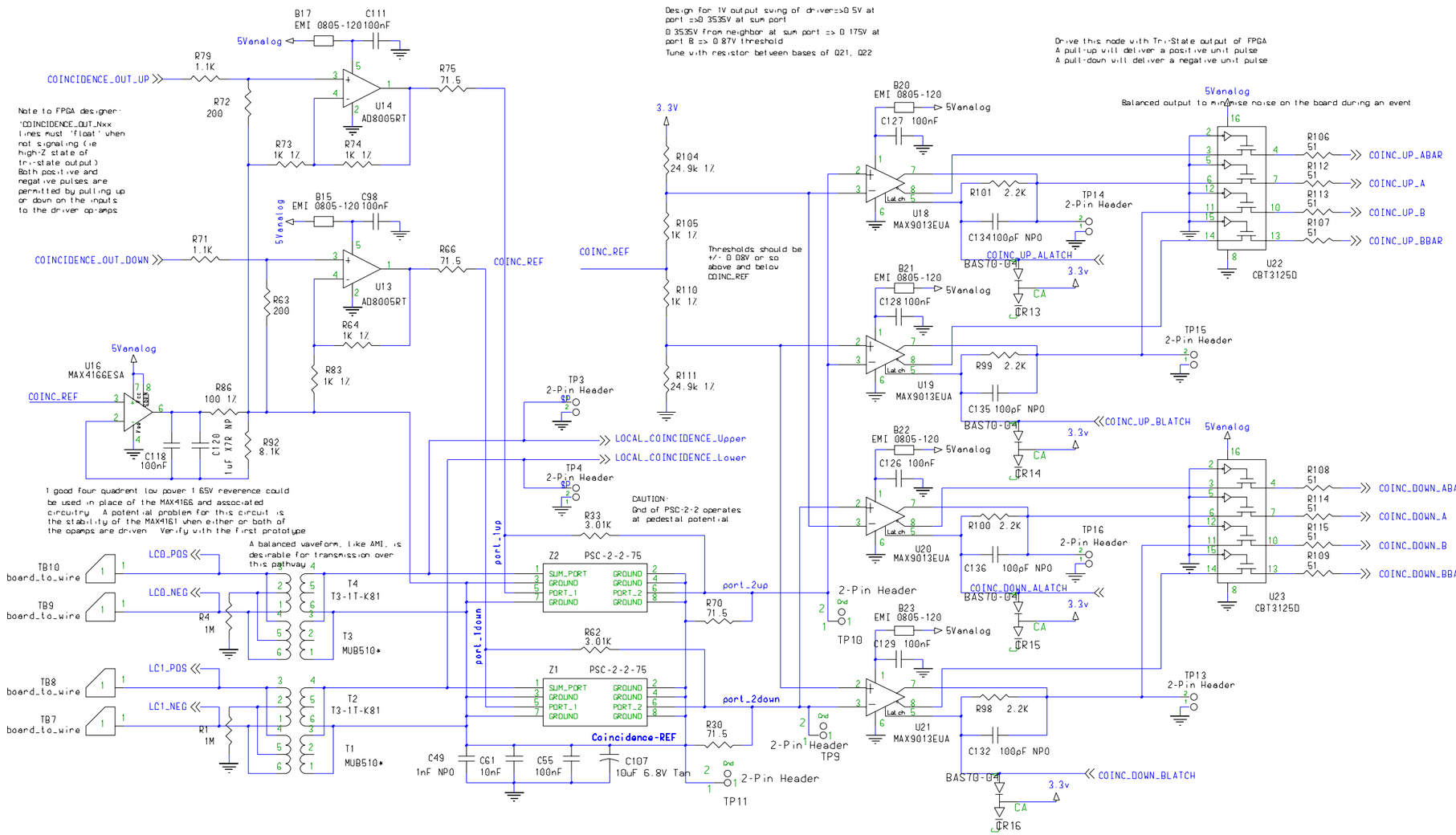


rhm 9/24 changed to EXSDIO for fixed resistors

CHECK PRINT 1/9/04

+ =DNL

Title	Digital Optical Module Memory	
Size: D	Document Number: main_board_vsn4.1 Sheet 7	Rev: 12.0
Date: Wednesday, October 09, 2002	Sheet 10 of 14	



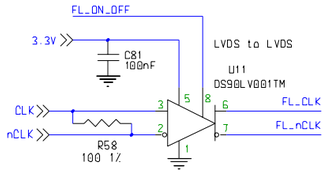
Power = 4*1.3*5 + 2*0.4*5 + 1*1.3*5 = 35 mW

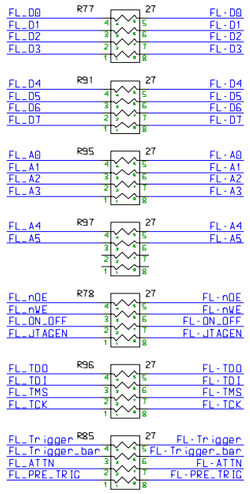
* = DNL

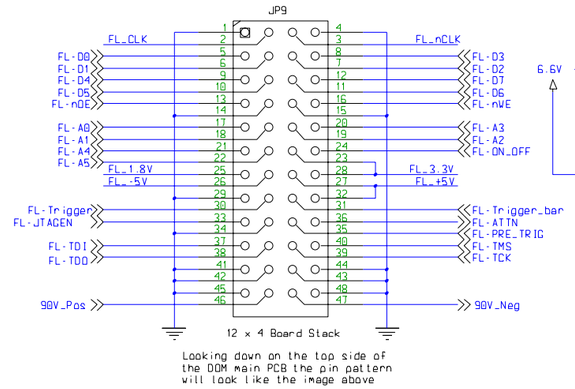
CHECK PRINT 1/9/04

Title	Digital Optical Module Local Coincidence		
Size C	Document Number main_board_vsn4.1 Sheet 8		Rev 12.0
Date: Wednesday, October 09, 2002	Sheet 9 of 14		

9/24 rhm change flsher pin 32 to +5v and pin 23 to 3.3V

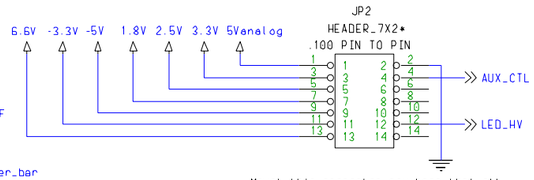




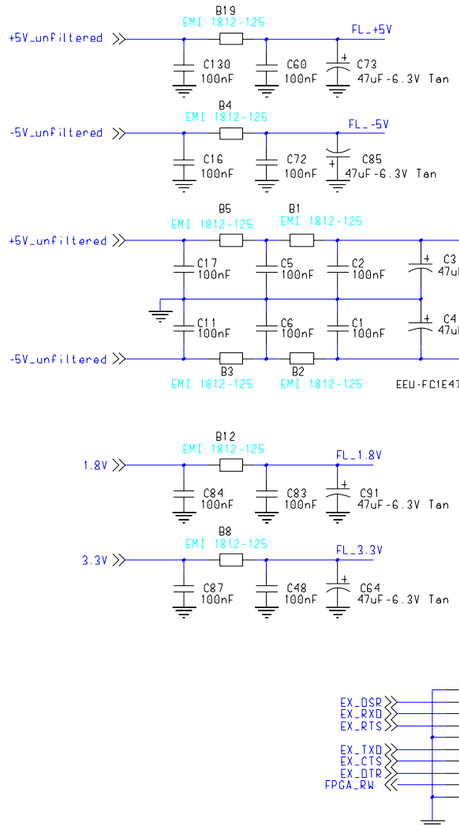


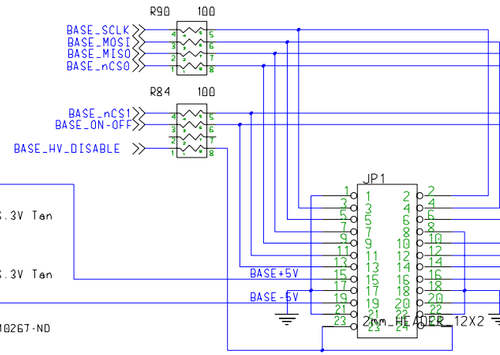
Looking down on the top side of the DOM main PCB the pin pattern will look like the image above

ESQT-112-02-L-Q-078



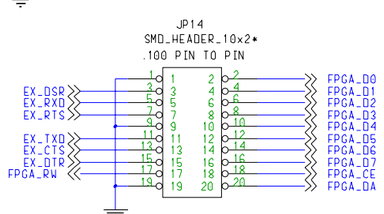
Mount this connector anywhere that all power supply voltages are available.

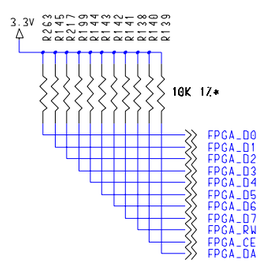




1 GND
2 SCK - Serial clock
3 SCK
4 MOSI -Serial data in
5 MOSI
6 MISO - Serial data out
7 MISO
8 GND
9 CS0 (DAC) - Chip select for DAC
10 CS0
11 CS1 (ADC) - Chip select for ADC
12 CS1
13 ON/OFF - Power supply enable/disable
14 ON/OFF
15 +5V - Main power
16 +5V
17 GND
18 GND
19 -5V - Main power
20 -5V

Should be STMM-112-02-S-D for EMCO base
Should be STMM-110-02-S-D for ISEG base
(24 pin for EMCO, 20 pin for ISEG)





* = DNL

CHECK PRINT 1/9/04

Title: Off-Board Subsystems		
Size: C	Document Number: main_board_vsn4.1 Sheet 9	Rev: 12.0
Date: Wednesday, October 09, 2002	Sheet 8 of 14	

Maybe this part should have 22.5mm LS if EF2225-NDor 27.5mm LS if E2225-ND (preferred)

L1 Delevan SP073-334
L2 Delevan SP073-334
Layout to avoid magnetic coupling
Cable+
Cable-
RV1 V120CH8
C9 10uF 160V Dearborn 730P106X9160
R2 10M
R3 10M
C152 470nF 250v
C15 470nF 250v
D1N3595US-1 Hrd glass CR23
B27 EMI 1812-125
B30 EMI 1812-125
C153 220uF-160V+ P4864-ND OPTIONAL
DC IN1
DC IN2
JP3
HEADER_7X2_shrouded
LC0_POS
LC1_POS
LC0_NEG
LC1_NEG
move to allow shrouded connector

TB4 board_to_wire
TB1 board_to_wire
TB3 board_to_wire
TB2 board_to_wire
C7 470nF 250v
tip-n-ring ceramic
C8 470nF 250v
tip-n-ring ceramic

5Vanalog
B9 EMI 0805-120
C69 100nF
COM+5
TP6 2-Pin Header
TP7 2-Pin Header
LINE_A
LINE_B
COMM-REF
5Vanalog
U10 AD8130AR*
+Vs
-Vs
+IN
-IN
PD*
REF
FB
OUT
R59 499 1/4
R54 2K 1/4
C88 Open Ckt
R60 Open Ckt
C75 100nF
B10 EMI 0805-120
-5V
Gain=(1+(1.4K/Rg))
Differential line receiver

C115 100nF
U17 AD830 10.8 mW
R87 20
COM_IN
Route COM_IN for minimal noise coupling from digital sources
C125 100nF
R93 499 1/
R94 2K 1/
C113 Open Ckt
R81 Open Ckt

5Vanalog 3.3V
R116 Open Ckt
R117 Open Ckt
C144 100nF
U26 sn65hvd114
sn65hvd11
Vdd
GND
HVD_Rx
HVD_RxENA
HVD_TxENA
HVD_IN
R
RE
DE
D
R124 open
R127 open
LINE_A
LINE_B
rs485 alternate driver

3.3V
C177 100nF
R190 20
COM_CLK
U33 DS90LV018ATM
CLK
nCLK
DS90LV018ATM

This part is located very near the FPGA. If possible return the ground for this part to the communications input circuit.
U39 AD9215BRU-65 100 mW
TP12 2-Pin Header
COM_IN
R67 20*
3.3V
C10 BAS70-04
R229 100 1/
R223 100 1/
COMM-REF
C197 Open Ckt
C196 Open Ckt
C226 100pF NPO*
VIN+
VIN-
OTR
CLK
PDWN
MODE
REFT
REFB
VREF
SENSE
DVdd
AVdd
AVdd
DGnd
AGnd
AGnd
D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11
R215 100 1/ COM_AD_D0
R214 100 1/ COM_AD_D1
R221 100 1/ COM_AD_D2
R220 100 1/ COM_AD_D3
R228 100 1/ COM_AD_D4
R227 100 1/ COM_AD_D5
R235 100 1/ COM_AD_D6
R224 100 1/ COM_AD_D7
R245 100 1/ COM_AD_D8
R244 100 1/ COM_AD_D9
R251 100 1/ COM_AD_D10
R250 100 1/ COM_AD_D11
R252 100 1/ COM_AD_OTR
COM_CLK
R204 38.3K 1/
3.3V
2.5V
EMI 0805-120
B39
C179 100nF
C178 100nF
Essential to clock the communications ADC at power up in order to communicate at all
With some switch fets and FPGA (or PLD) control lines, one could cause the span to be controlled remotely. 1V span may be good for digitizing time ticks. If pins are lacking, then, perhaps 1V span should be chosen to reduce constraints on the input amplifier.
C234 10uF 6.8V Tan
C203 100nF
C236 100nF
C213 100nF
C229 100nF
Open Ckt
C247 10uF 6.8V Tan
JU6
JU7
Jumper
COM_AD_REF
R223 Ra*
R248 Rb*
Strap SENSE to Gnd for 2V Span
Strap SENSE to VREF for 1V span
Strap SENSE to Voltage Divider for span of (Rt+Rb/Rb)

JP16 2 Pin Header
R171 200 Size 1210
up to 150 mW
5Vanalog
3.3V
3.3V
B32 EMI 0805-120* DO NOT LOAD
B33 EMI 0805-120
B31 EMI 0805-120
U32 AD9708AR
IOUTA
IOUTB
COMP2
COMP1
FSADJ
REFIO
REFLO
AVDD
DVDD
ACOM
DCOM
CLK
SLEEP
DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7 DB8 DB9 DB10 DB11 DB12 DB13
COM_AD0 COM_AD1 COM_AD2 COM_AD3 COM_AD4 COM_AD5 COM_AD6 COM_AD7 COM_AD8 COM_AD9 COM_AD10 COM_AD11 COM_AD12 COM_AD13
COM_CLK
COM_TX_SLEEP
R209 2K 1/
Possible upgrade to AD9754AR
R182 Jumper
R181 Jumper
C174 10pF NPO*
REFIO
C171 10uF 6.8V Tan
C167 OSCON_6SEP82M
R183 2K 1/
C176 100nF
C173 100nF
C170 100nF
C186 100nF
C166 100nF

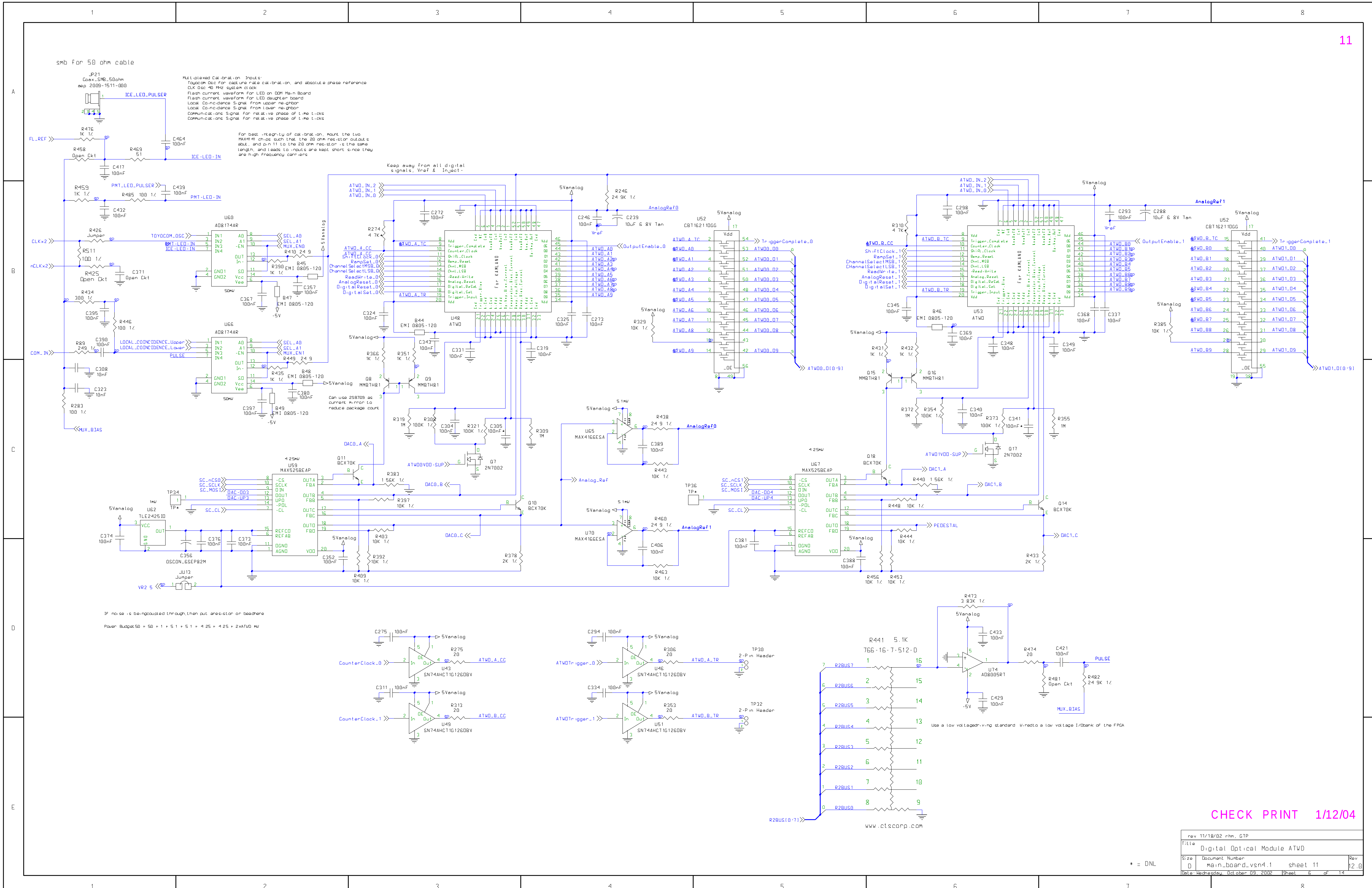
Replace CR7, CR8 with 5V zener diodes
5Vanalog
R25 Open Ckt
R27 Jumper
CR4 MMBD4448HTS
CR6 MMBD4448HTS
CR7 MMBD4448HTS
CR5 MMBD4448HTS
CR3 MMBD4448HTC*
3.3V
T5 TT1.5-6-KK81
T6 MLP-2012
R19 1M
R16 1M
R28 1M
JP5 2 Pin Header
R8 140

REFIO
R76 5.11K 1/
U15 MAX416GESA
R82 24.9 1/
R80 Open Ckt
R65 10K 0.1/
C100 1uF X7R NP
available from garrett
1.0V +/- Voffset of MAX4166
C101 100nF
5.2 mW
C119 100nF
C117 10uF 6.8V Tan
COMM-REF

* = DNL

CHECK PRINT 1/12/04

rev 11/13/02 rhm gtp rs485 driver added
rev 12/10/02 rhm subs ad830 for ad8130
Title: Digital Optical Module Communication
Size: C | Document Number: main_board_vsn4.1 | sheet 10 | Rev
Date: Wednesday, October 09, 2002 | Sheet 7 of 14


11
smb for 50 ohm cable
Multiplexed Calibration Inputs:
Toyocom Osc for capture rate calibration, and absolute phase reference
CLK Osc 40 MHz system clock
Flash current waveform for LED on DOM Main Board
Flash current waveform for LED daughter board
Local Coincidence Signal from upper neighbor
Local Coincidence Signal from lower neighbor
Communications Signal for relative phase of time ticks
Communications Signal for relative phase of time ticks
For best integrity of calibration, mount the two MAX4141 chips such that the 20 ohm resistor outputs abut, and pin 11 to the 20 ohm resistor is the same length, and leads to inputs are kept short since they are high frequency carriers
Keep away from all digital signals, Vref & Inject.
Can use 2SB709 as current mirror to reduce package count
If noise is beingcoupled through,then put aresistor or beadhere
Power Budget50 + 50 + 1 + 5 1 + 5 1 + 4 25 + 4 25 + 2xATWD mW
Use a low voltagedriving standard. Wiredto a low voltage I/Obank of the FPGA
www.ctscorp.com
CHECK PRINT 1/12/04
* = DNL
rev 11/18/02 rhm, GTP
Title
Digital Optical Module ATWD
Size D
Document Number main_board_vsn4.1 sheet 11
Rev 12.0
Date: Wednesday, October 09, 2002
Sheet 6 of 14

U50
EXCALIBUR_X41B
IO_Bank_12
IO_Bank 12 not including multi-purpose pins
EPXA1F67212

DO NOT CHANGE PINASSIGNMENTS OF AC8, AD7, AD8, AE7
These pin assignments chosen to optimize speed gtp9/11/02

R2261 100 1/
R2277 100 1/
R2280 100 1/
R2295 100 1/
C268 22pF NPO
C280 22pF NPO
C290 22pF NPO
C299 22pF NPO
COINC_UP_A
COINC_UP_B
COINC_DOWN_A
COINC_DOWN_B
COINC_UP_ABAR
COINC_UP_BBAR
COINC_DOWN_ABAR
COINC_DOWN_BBAR
Terminations, placed near FPGA

U50
EXCALIBUR_X41A
I/O Bank 13
I/O Bank 13 not including multi-purpose pins
R2257 100 1/
EPXA1F67212

U50
EXCALIBUR_X41F
IO_Bank_8
EPXA1F67212

U50
EXCALIBUR_X41H
IO_Bank_6
IO_Bank_6 Extension Bus Interface
See Errata
EPXA1F67212
EB_nCS0 R406 4.7K
EB_nCS1 R408 4.7K
EB_nCS2 R407 4.7K
EB_nCS3 R405 4.7K
3.3V
Flash Chip Select routed through PLD
BE not needed with 16 bit wide memory

U50
EXCALIBUR_X41K
IO_Bank_2
IO_Bank_2 SD RAM Bus
EPXA1F67212
SD_nCLK must make a loop of approx same length as SD_CLK to match timing
See HW Ref Manual

If the FE_TEST_PULSE line injects objectionable noise into the front, then perhaps that could be mitigated by making it drive differentially → ATWDTrigger_0

U50
EXCALIBUR_X41C
IO_Bank 11
EPXA1F67212

U50
EXCALIBUR_X41E
IO_Bank 9
IO_Bank 9 not including multi-purpose pins
R415 100 1/
R2BUS0 R2BUS1 R2BUS2 R2BUS3 R2BUS4 R2BUS5 R2BUS6 R2BUS7 R2BUS[0:7]
FE_TEST_PULSE
OneSPE_nL
COMM_DB0
COMM_DB1
FLASH_AD_D0
COMM_RESET
COMM_DB2
FPGA_LOADED
COMM_DB3
FPGA_R4
FE_PULSER0p FE_PULSER0n FE_PULSER1p FE_PULSER1n FE_PULSER2p FE_PULSER2n FE_PULSER3p FE_PULSER3n
PLD_FPGA_nOE PLD_FPGA_nWE PLD_FPGA_BUSY
PLD_FPGA_[0:7]
EPXA1F67212

R404 10K 1/
R411 10K 1/
ATWD1VDD-SUP
ATWD0VDD-SUP

U50
EXCALIBUR_X41D
IO_Bank 10
IO_Bank 10 not including multi-purpose pins
TriggerComplete_0 OutputEnable_0 CounterClock_0 ShiftClock_0 RampSet_0 ChannelSelectMSB_0 ChannelSelectLSB_0 ReadWrite_0 AnalogReset_0 DigitalReset_0 DigitalSet_0
ATWD0_D0 ATWD0_D1 ATWD0_D2 ATWD0_D3 ATWD0_D4 ATWD0_D5 ATWD0_D6 ATWD0_D7 ATWD0_D8 ATWD0_D9 ATWD0_D[0:9]
TriggerComplete_1 OutputEnable_1 CounterClock_1 ShiftClock_1 RampSet_1 ChannelSelectMSB_1 ChannelSelectLSB_1 ReadWrite_1 AnalogReset_1 DigitalReset_1 DigitalSet_1
ATWD1_D0 ATWD1_D1 ATWD1_D2 ATWD1_D3 ATWD1_D4 ATWD1_D5 ATWD1_D6 ATWD1_D7 ATWD1_D8 ATWD1_D9 ATWD1_D[0:9]
3.3V
10K 1/
EPXA1F67212

U50
EXCALIBUR_X41M
NC
EPXA1F67212

Connect all the NO_CONNECT pins to an obstacle on a plane that WILL NOT map to a gerber layer This insures that all the pins are connected to pads, so are accessable

FE_PULSER0p FE_PULSER1p FE_PULSER2p FE_PULSER3p FE_PULSER3n FE_PULSER2n FE_PULSER1n FE_PULSER0n
R302 R299 R300 R298 R284 R285 R286 R288 200
R273 R268 R272 R292 R291 R269 100
R287 R301 200
R192 51
R206 51
LONG TRACES OK ROUTE AS A PAIR
T8 T1-6-KK81
T7 MUB55*
R198 1
Vref
Inject-
TP24 TP*

U50
EXCALIBUR_X41L
GND
VccInt
VccIO
VccCKLK
VccCKOUT
EPXA1F67212
1.8V
C351 OSCON_6SEP82M
C411 OSCON_6SEP82M
From Sanyo Video
C264 470pF NPO
C300 470pF NPO
C326 100nF
C366 100nF
C365 470pF NPO
C214 OSCON_6SEP82M
C264 100nF
C286 470pF NPO
C436 OSCON_6SEP82M
C265 100nF
C267 470pF NPO
C194 OSCON_6SEP82M
C259 100nF
C258 470pF NPO
C382 OSCON_6SEP82M
C260 100nF
C262 470pF NPO
C393 OSCON_6SEP82M
C263 100nF
C295 470pF NPO
C437 OSCON_6SEP82M
C322 100nF
C270 470pF NPO
C155 OSCON_6SEP82M
C306 100nF
C266 470pF NPO
C457 OSCON_6SEP82M
C156 100nF
C261 470pF NPO
C335 OSCON_6SEP82M
C165 100nF
C254 470pF NPO
C383 OSCON_6SEP82M
C271 100nF
EXSDIO
R427 Open Ckt
R428 Open Ckt
R429 Jumper
3.3V
2.5V
1.8V
EXSDIO (POWER PLANE/FILL)
I/O bank used by SDRAM Support options I/O voltages
R271 Open Ckt
R279 Open Ckt
R281 Open Ckt
R289 Open Ckt
R315 Open Ckt
R421 Open Ckt
R420 Open Ckt
R419 Jumper
(POWER PLANE/FILL)
MEMVIO
Place smallest capacitor nearest to FPGA
VddC8
VddC0
Wide & short traces to bypass caps
C232 10nF C210 100nF C221 10uF 6.8V Tan R37 EMI 1812-125 1.8V
C222 2.2uF 6.3V Tan
C244 10nF C243 100nF C269 10uF 6.8V Tan B34 EMI 1812-125
C228 2.2uF 6.3V Tan
C297 10nF C282 100nF C291 10uF 6.8V Tan B41 EMI 1812-125
C289 2.2uF 6.3V Tan
C233 10nF C211 100nF C217 10uF 6.8V Tan B38 EMI 1812-125
C223 2.2uF 6.3V Tan
C231 10nF C209 100nF C219 10uF 6.8V Tan B36 EMI 1812-125
C220 2.2uF 6.3V Tan

CHECK PRINT 1/9/04

* = DNL

rev 11/18/02 rhm/ gtp	
Title	Digital Optical Module FPGA sheet
Size D	Document Number main_board_vsn4 1 Rev 12 0
Date: Wednesday, October 09, 2002	Sheet 5 of 14

Per criterion established July 2002 (global rm) the design goal for the IceCube DOM is 200 PE = 1V into the ATWD dictated by PMT saturation behavior. Namely, the PMT NEVER delivers more than about 2V, and is linear to about 1V into a 50 ohm load (100 ohm || back-termination)

Locate these amplifiers --> close to the PMT signal input

1x1 3x5 = 2x1 3x5 = 6.8x10 = 2x1 15x10x2x1 1x5= 3x0.4x10.1x34mw
opamp comparator, 1135 8014 8014 8005

AD advertises that these (400 MHz) amplifiers recover in 60 ns. At 5 mV per stage, they give slightly less performance than an HA1135 at 1/10th the current. Saturation is not a big issue for the (latching) comparator input, since latch recovery is controlled by the FPGA

If we have power to burn, once all revisions are taken into account, the 850 MHz bandwidth HA1135 may prove to be a better choice as comparator input amplifier, as one stage should have less delay than 2

The comparators exhibit less trigger delay if driven by a positive signal, so the second gain stage inverts. The first one buffers to minimize load on the PMT signal

If test pulser, U52, injects too much power supply noise, it will have to go, in favor of something that is quieter

Caution: the comparators are 5V parts that cannot be operated from 3.3V. Care must be taken to protect the driven 3.3V part

Calibration input test point. Drive with 5V square wave to generate fixed amplitude test pulses

Route FE_TEST_PULSE away from sensitive analog circuits and ATWD inputs

JP5 located at -4.432, -2.559 oriented 210 degrees with pins 1& 2 near outer edge

If the PMT delivers 3V into a 50 ohm load, then change the divider resistors to R30=31.7, and R54=63.4. Leave the gain of the amplifier unchanged. The design goal is to have the PMT saturation voltage within the span of the ATWD

Test pulse injection if it doesn't work, remove transformer, and use jumper 1

Minimize trace length to the inverting input of opamps. Remove inner power plane layers a min. of 2mm from any trace or pad connected to the inverting input of high speed opamps

The shaped signal path design was from Harold Yaver and the Engineering Department -Modifications added to insure stable offset behavior, and to offset the output to match the input range of the ADC

gnd pad near JP4

X3.0

X5.33

X2

1/8

X16

CHECK PRINT 1/9/04

* = DNL

title	Digital Optical Module Analog Front End
	GTP/JL/DRN/HY
Size	D
Document Number	main_board_vsn4.1
Rev	12.0
Date	Wednesday, October 09, 2002
Sheet	13 of 14

Since the sensor uses about 60mW, it would be prudent to disable power to it when not needed

It remains to be seen how prudent it is to float the ground lead. The alternative may be a P-FET in the Vcc enabled by the N-FET

TI claims to have a lower power part, but only accurate to 2 deg C (probably within the -25C and above range)

-(-5/2.5)·(+3.3+2.5+1.8)/4 =Vout
2 · 0.825 · 0.625 · 0.450) = 0.100V
Lets just assume that if +5 is gone, we're dead. The 5V CPU supervisory chip input will cause reboot below about 4.750V

Vout=Vs(0.009*P-0.095)+/-Error
P = 111.1111111*Vs+Vout*10.55555556
5V and Baro are scaled by the same factor, so are in the same units

Place resistors near remote sources. Capacitors near ADC

Place resistors near remote sources. Capacitors near ADC

Route DAC & ADC control signals around power supply side of the board

4.25 mW x 4 + 7.5mW = 24.5 mWplus 3.3mW when converting temperature 6mW x 10V/conv_eff = 67 mW

If we can use the 2.5V reference output of the ADC, then we can eliminate the TLE2425 reference chip

The (differential input) 40 MHz ADC non inverting input, used as the center-scale reference

Part values ending in "*" should not be mounted. These part are for diagnostics or implementation of alternate methodologies

Note that this FADC is differential input. Amplifier and shaper stages are DC coupled. The 'bottom' of the span depends on the setting of the ATWD pedestal voltage. I.e., Pedestal for the FADC = Pedestal for the ATWD. Vt in must be set to (Vpedestal - (span/2)) volts, or a few mV lower

A 10uF Tantalum capacitor is needed on U4-1 to insure stability. gtp 4/13/99

Components whose value ends in "*" are not to be mounted

Strap SENSE to Gnd for 2V Span. Strap SENSE to VREF for 1V span. Strap SENSE to Voltage Divider for span=1.0(1+Ra/Rb)

CHECK PRINT 1/9/04

* = DNL

Title	Digital Optical Module AD/DA		
Size C	Document Number main_board_vsn4.1 Sheet 14		Rev 12.0
Date: Wednesday, October 09, 2002	Sheet 3 of 14		