Tek Run: 2.50GS/s   Average

△: 46.8ns
@: 43.4ns

C2→C1 Dly
1.08ns
Low signal
amplitude

C2→C3 Dly
28.90ns
Low signal
amplitude

C2→C4 Dly
28.62ns
Low signal
amplitude

C3→C4 Dly
−300ps
Low signal
amplitude

Ch1 2.00 V   Ch2 2.00 V   M 10.0ns Ch2 ∫ 600mV
Ch3 2.00 V   Ch4 2.00 V

gtp LBNL
7 Mar 2006
17:35:08

CH1: 20 MHz ADC Clock on DOR card
CH2: 10 MHz Refference from GPS clock
CH3: 20 MHz ADC Clock from DOM A Under Test
CH4: 20 MHz ADC Clock from DOM B Under Test
Positive phase shift corresponds to right shift of DOM ADC clock