



3.3-V RS-485 TRANSCEIVERS

FEATURES

- Operates With a 3.3-V Supply
- Bus-Pin ESD Protection Exceeds 16 kV HBM
- 1/8 Unit-Load Option Available (Up to 256 Nodes on the Bus)
- Optional Driver Output Transition Times for Signaling Rates† of 1 Mbps, 10 Mbps and 25 Mbps
- Meets or Exceeds the Requirements of ANSI TIA/EIA-485-A
- Bus-Pin Short Circuit Protection From –7 V to 12 V
- Low-Current Standby Mode . . . 1 μ A Typical
- Open-Circuit and Shorted-Bus Failsafe Receiver
- Thermal Shut-Down Protection
- Glitch-Free Power-Up and Power-Down Protection for Hot-Plugging Applications
- SN75176 Footprint

APPLICATIONS

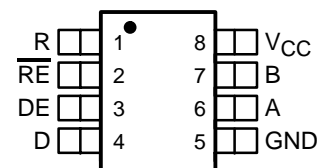
- Digital Motor Control
- Utility Meters
- Chassis-to-Chassis Interconnects
- Electronic Security Stations
- Industrial Process Control
- Building Automation
- Point-of-Sale (POS) Terminals and Networks

DESCRIPTION

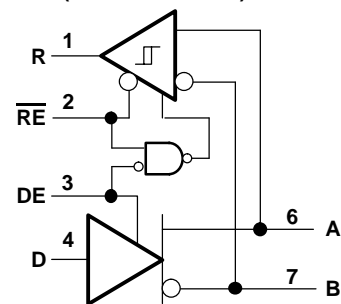
The SN65HVD10, SN75HVD10, SN65HVD11, SN75HVD11, SN65HVD12, and SN75HVD12 combine a 3-state differential line driver and differential input line receiver that operate with a single 3.3-V power supply. They are designed for balanced transmission lines and meet or exceed ANSI standard TIA/EIA-485-A and ISO 8482:1993. These differential bus transceivers are monolithic integrated circuits designed for bidirectional data communication on multipoint bus-transmission lines. The drivers and receivers have active-high and active-low enables respectively, that can be externally connected together to function as direction control. Very low device standby supply current can be achieved by disabling the driver and the receiver.

The driver differential outputs and receiver differential inputs connect internally to form a differential input/output (I/O) bus port that is designed to offer minimum loading to the bus whenever the driver is disabled or $V_{CC} = 0$. These parts feature wide positive and negative common-mode voltage ranges, making them suitable for party-line applications.

D OR P PACKAGE
(TOP VIEW)



LOGIC DIAGRAM
(POSITIVE LOGIC)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

†The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

SIGNALING RATE	UNIT LOADS	T _A	PACKAGE		SOIC MARKING
			SOIC(1)	PDIP	
25 Mbps	1/2	-40°C to 85°C	SN65HVD10D	SN65HVD10P	VP10
10 Mbps	1/8		SN65HVD11D	SN65HVD11P	VP11
1 Mbps	1/8		SN65HVD12D	SN65HVD12P	VP12
25 Mbps	1/2	-0°C to 70°C	SN75HVD10D	SN75HVD10P	VN10
10 Mbps	1/8		SN75HVD11D	SN75HVD11P	VN11
1 Mbps	1/8		SN75HVD12D	SN75HVD12P	VN12
25 Mbps	1/2	-40°C to 125°C	SN65HVD10QD		VP10Q
10 Mbps	1/8		SN65HVD11QD		VP11Q

(1) The D package is available taped and reeled. Add an R suffix to the part number (i.e., SN75HVD11DR).

PACKAGE DISSIPATION RATINGS

PACKAGE	T _A ≤ 25°C POWER RATING	DERATING FACTOR(1) ABOVE T _A = 25°C	T _A = 70°C POWER RATING	T _A = 85°C POWER RATING	T _A = 125°C POWER RATING
D(2)	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
D(3)	1282 mW	10.3 mW/°C	822 mW	667 mW	255 mW
P	1150 mW	9.2 mW/°C	736 mW	598 mW	–

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

(2) Tested in accordance with the Low-K thermal metric definitions of EIA/JESD51–3.

(3) Tested in accordance with the High-K thermal metric definitions of EIA/JESD51–7.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1) (2)

		SN65HVD10, SN75HVD10 SN65HVD11, SN75HVD11 SN65HVD12, SN75HVD12
Supply voltage range, V _{CC}		-0.3 V to 6 V
Voltage range at A or B		-9 V to 14 V
Input voltage range at D, DE, R or \overline{RE}		-0.5 V to V _{CC} + 0.5 V
Voltage input range, transient pulse, A and B, through 100 Ω (see Figure 11)		-50 V to 50 V
Electrostatic discharge	Human body model(3)	A, B and GND 16 kV All pins 4 kV
	Charged-device model(4)	All pins Charge 1 kV
Continuous total power dissipation		See Dissipation Rating Table
Storage temperature range, T _{stg}		-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

(3) Tested in accordance with JEDEC Standard 22, Test Method A114-A.

(4) Tested in accordance with JEDEC Standard 22, Test Method C101.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		3		3.6	V
Voltage at any bus terminal (separately or common mode) V_I or V_{IC}		-7 ⁽¹⁾		12	V
High-level input voltage, V_{IH}	D, DE, \overline{RE}	2		V_{CC}	V
Low-level input voltage, V_{IL}	D, DE, \overline{RE}	0		0.8	V
Differential input voltage, V_{ID} (see Figure 7)		-12		12	V
High-level output current, I_{OH}	Driver	-60			mA
	Receiver	-8			
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Operating free-air temperature, T_A	SN65HVD10Q ⁽²⁾	-40		125	°C
	SN65HVD11Q ⁽²⁾				
	SN65HVD10	-40		85	°C
	SN65HVD11				
	SN65HVD12				
	SN75HVD10	0		70	°C
	SN75HVD11				
SN75HVD12					

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

(2) Product Preview

DRIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -18$ mA		-1.5			V
$ V_{OD} $	Differential output voltage	$I_O = 0$		2		V_{CC}	V
		$R_L = 54 \Omega$, See Figure 1		1.5			
		$V_{test} = -7$ V to 12 V, See Figure 2		1.5			
$\Delta V_{OD} $	Change in magnitude of differential output voltage	See Figure 1 and Figure 2		-0.2		0.2	V
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage	See Figure 3			400		mV
$V_{OC(SS)}$	Steady-state common-mode output voltage			1.4		2.5	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage			-0.05		0.05	V
I_{OZ}	High-impedance output current	See receiver input currents					
I_I	Input current	D		-100		0	μ A
		DE		0		100	
I_{OS}	Short-circuit output current	-7 V $\leq V_O \leq 12$ V		-250		250	mA
$C_{(OD)}$	Differential output capacitance	$V_{OD} = 0.4 \sin(4E6\pi t) + 0.5$ V, DE at 0 V			16		pF
I_{CC}	Supply current	\overline{RE} at V_{CC} , D & DE at V_{CC} , No load	Receiver disabled and driver enabled		9	15.5	mA
		\overline{RE} at V_{CC} , D at V_{CC} , DE at 0 V, No load	Receiver disabled and driver disabled (standby)		1	5	μ A
		\overline{RE} at 0 V, D & DE at V_{CC} , No load	Receiver enabled and driver enabled		9	15.5	mA

(1) All typical values are at 25°C and with a 3.3-V supply.

DRIVER SWITCHING CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t _{PLH}	Propagation delay time, low-to-high-level output	HVD10	5	8.5	16	ns
		HVD11	18	25	40	
		HVD12	135	200	300	
t _{PHL}	Propagation delay time, high-to-low-level output	HVD10	5	8.5	16	ns
		HVD11	18	25	40	
		HVD12	135	200	300	
t _r	Differential output signal rise time	HVD10	3	4.5	10	ns
		HVD11	10	20	30	
		HVD12	100	170	300	
t _f	Differential output signal fall time	HVD10	3	4.5	10	ns
		HVD11	10	20	30	
		HVD12	100	170	300	
t _{sk(p)}	Pulse skew (t _{PHL} – t _{PLH})	HVD10			1.5	ns
		HVD11			2.5	
		HVD12			7	
t _{sk(pp)} ⁽²⁾	Part-to-part skew	HVD10			6	ns
		HVD11			11	
		HVD12			100	
t _{PZH}	Propagation delay time, high-impedance-to-high-level output	HVD10			31	ns
		HVD11			55	
		HVD12			300	
t _{PHZ}	Propagation delay time, high-level-to-high-impedance output	HVD10			25	ns
		HVD11			55	
		HVD12			300	
t _{PZL}	Propagation delay time, high-impedance-to-low-level output	HVD10			26	ns
		HVD11			55	
		HVD12			300	
t _{PLZ}	Propagation delay time, low-level-to-high-impedance output	HVD10			26	ns
		HVD11			75	
		HVD12			400	
t _{PZH}	Propagation delay time, standby-to-high-level output	R _L = 110 Ω, \overline{RE} at 3 V, See Figure 5			6	μs
t _{PZL}	Propagation delay time, standby-to-low-level output	R _L = 110 Ω, \overline{RE} at 3 V, See Figure 6			6	μs

(1) All typical values are at 25°C and with a 3.3-V supply.

(2) t_{sk(pp)} is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	$I_O = -8 \text{ mA}$			-0.01	V
V_{IT-}	Negative-going input threshold voltage	$I_O = 8 \text{ mA}$	-0.2			
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)			35		mV
V_{IK}	Enable-input clamp voltage	$I_I = -18 \text{ mA}$	-1.5			V
V_{OH}	High-level output voltage	$V_{ID} = 200 \text{ mV}$, $I_{OH} = -8 \text{ mA}$, See Figure 7	2.4			V
V_{OL}	Low-level output voltage	$V_{ID} = -200 \text{ mV}$, $I_{OL} = 8 \text{ mA}$, See Figure 7			0.4	V
I_{OZ}	High-impedance-state output current	$V_O = 0 \text{ or } V_{CC}$, \overline{RE} at V_{CC}	-1		1	μA
I_I	Bus input current	$V_A \text{ or } V_B = 12 \text{ V}$	HVD11, HVD12, Other input at 0 V	0.05	0.11	mA
		$V_A \text{ or } V_B = 12 \text{ V}$, $V_{CC} = 0 \text{ V}$		0.06	0.13	
		$V_A \text{ or } V_B = -7 \text{ V}$		-0.1	-0.05	
		$V_A \text{ or } V_B = -7 \text{ V}$, $V_{CC} = 0 \text{ V}$		-0.05	-0.04	
		$V_A \text{ or } V_B = 12 \text{ V}$	HVD10, Other input at 0 V	0.2	0.5	mA
		$V_A \text{ or } V_B = 12 \text{ V}$, $V_{CC} = 0 \text{ V}$		0.25	0.5	
		$V_A \text{ or } V_B = -7 \text{ V}$		-0.4	-0.2	
		$V_A \text{ or } V_B = -7 \text{ V}$, $V_{CC} = 0 \text{ V}$		-0.4	-0.15	
I_{IH}	High-level input current, \overline{RE}	$V_{IH} = 2 \text{ V}$	-30		0	μA
I_{IL}	Low-level input current, \overline{RE}	$V_{IL} = 0.8 \text{ V}$	-30		0	μA
C_{ID}	Differential input capacitance	$V_{ID} = 0.4 \sin(4E6\pi t) + 0.5 \text{ V}$, DE at 0 V		15		pF
I_{CC}	Supply current	\overline{RE} at 0 V, D & DE at 0 V, No load	Receiver enabled and driver disabled	4	8	mA
		\overline{RE} at V_{CC} , D at V_{CC} , DE at 0 V, No load	Receiver disabled and driver disabled (standby)	1	5	μA
		\overline{RE} at 0 V, D & DE at V_{CC} , No load	Receiver enabled and driver enabled	9	15.5	mA

(1) All typical values are at 25°C and with a 3.3-V supply.

RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT	
t _{PLH}	Propagation delay time, low-to-high-level output	HVD10	V _{ID} = -1.5 V to 1.5 V, C _L = 15 pF, See Figure 8	12.5	20	25	ns	
t _{PHL}	Propagation delay time, high-to-low-level output	HVD10		12.5	20	25		
t _{PLH}	Propagation delay time, low-to-high-level output	HVD11 HVD12		30	55	70	ns	
t _{PHL}	Propagation delay time, high-to-low-level output	HVD11 HVD12		30	55	70		
t _{sk(pp)}	Pulse skew (t _{PHL} - t _{PLH})	HVD10					1.5	ns
		HVD11					4	
		HVD12				4		
t _{sk(pp)} ⁽²⁾	Part-to-part skew	HVD10				8	ns	
		HVD11				15		
		HVD12				15		
t _r	Output signal rise time		C _L = 15 pF, See Figure 8	1	2	5	ns	
t _f	Output signal fall time			1	2	5		
t _{PZH(1)}	Output enable time to high level		C _L = 15 pF, DE at 3 V, See Figure 9			15	ns	
t _{PZL(1)}	Output enable time to low level					15		
t _{PHZ}	Output disable time from high level					20		
t _{PLZ}	Output disable time from low level					15		
t _{PZH(2)}	Propagation delay time, standby-to-high-level output		C _L = 15 pF, DE at 0, See Figure 10			6	μs	
t _{PZL(2)}	Propagation delay time, standby-to-low-level output					6		

(1) All typical values are at 25°C and with a 3.3-V supply.

(2) t_{sk(pp)} is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

PARAMETER MEASUREMENT INFORMATION

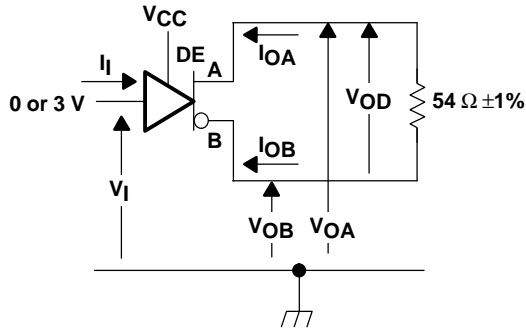


Figure 1. Driver V_{OD} Test Circuit and Voltage and Current Definitions

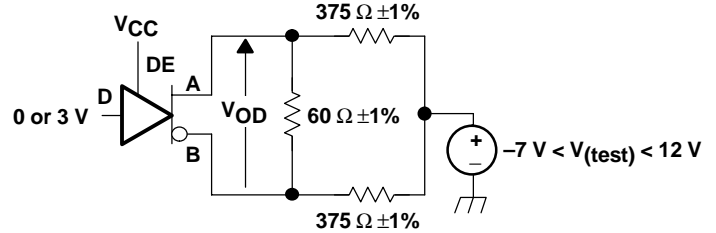
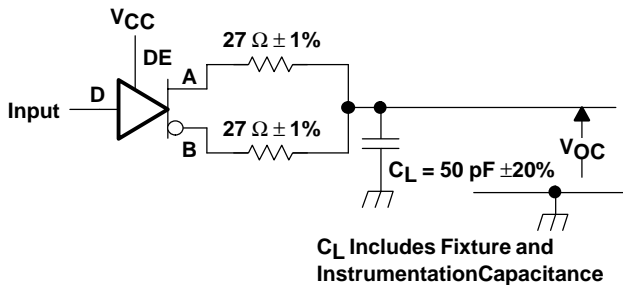
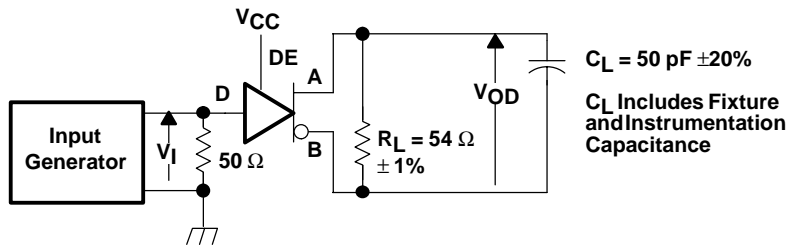
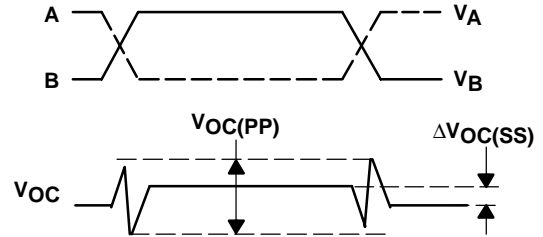


Figure 2. Driver V_{OD} With Common-Mode Loading Test Circuit



Input: PRR = 500 kHz, 50% Duty Cycle, $t_r < 6$ ns, $t_f < 6$ ns, $Z_0 = 50 \Omega$

Figure 3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage



Generator: PRR = 500 kHz, 50% Duty Cycle, $t_r < 6$ ns, $t_f < 6$ ns, $Z_0 = 50 \Omega$

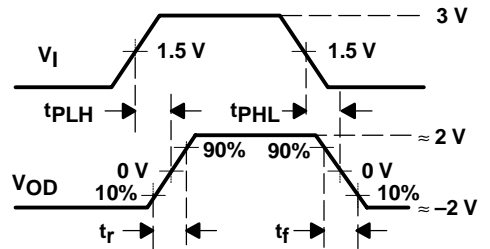


Figure 4. Driver Switching Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

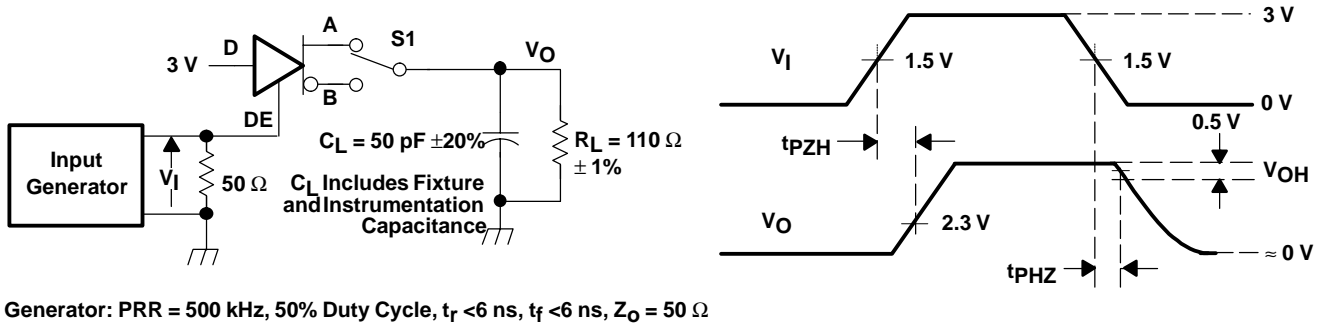


Figure 5. Driver High-Level Enable and Disable Time Test Circuit and Voltage Waveforms

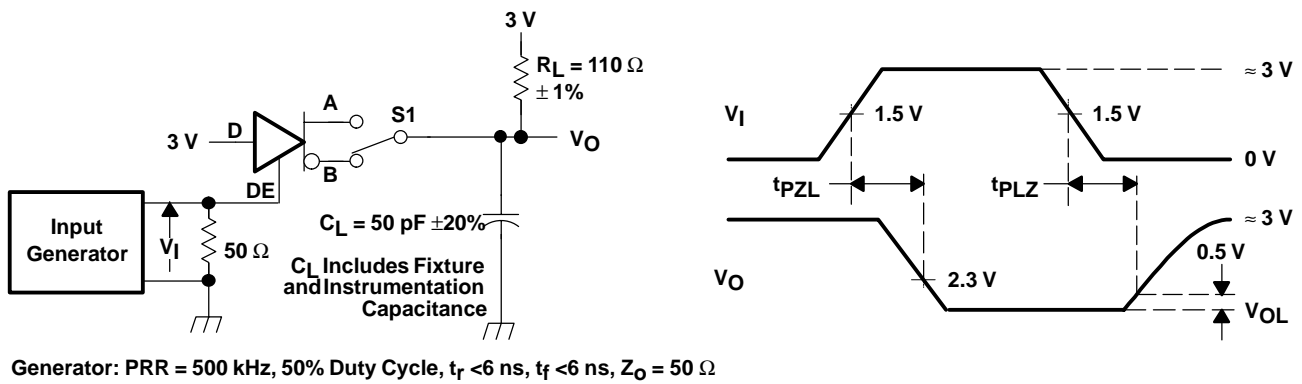


Figure 6. Driver Low-Level Output Enable and Disable Time Test Circuit and Voltage Waveforms

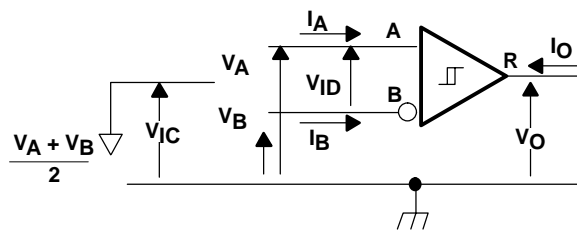
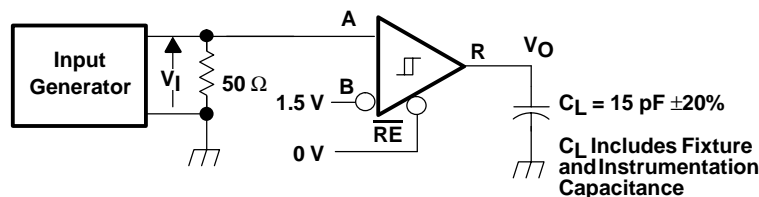


Figure 7. Receiver Voltage and Current Definitions

PARAMETER MEASUREMENT INFORMATION



Generator: PRR = 500 kHz, 50% Duty Cycle, $t_r < 6\ \text{ns}$, $t_f < 6\ \text{ns}$, $Z_0 = 50\ \Omega$

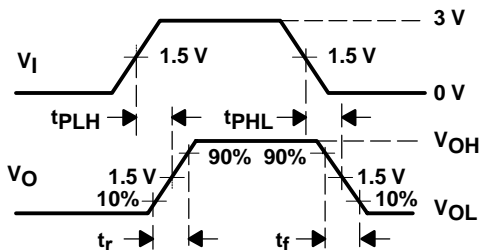
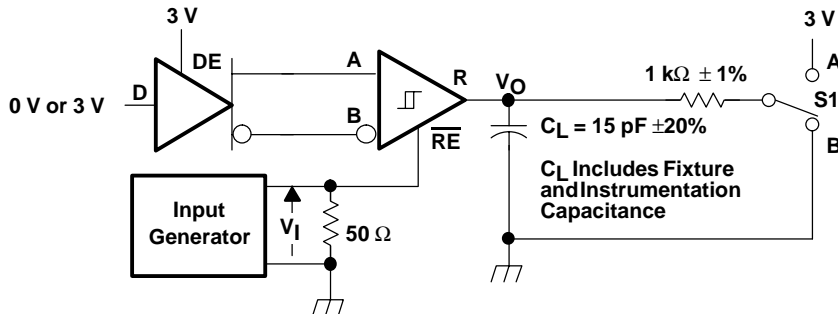


Figure 8. Receiver Switching Test Circuit and Voltage Waveforms



Generator: PRR = 500 kHz, 50% Duty Cycle, $t_r < 6\ \text{ns}$, $t_f < 6\ \text{ns}$, $Z_0 = 50\ \Omega$

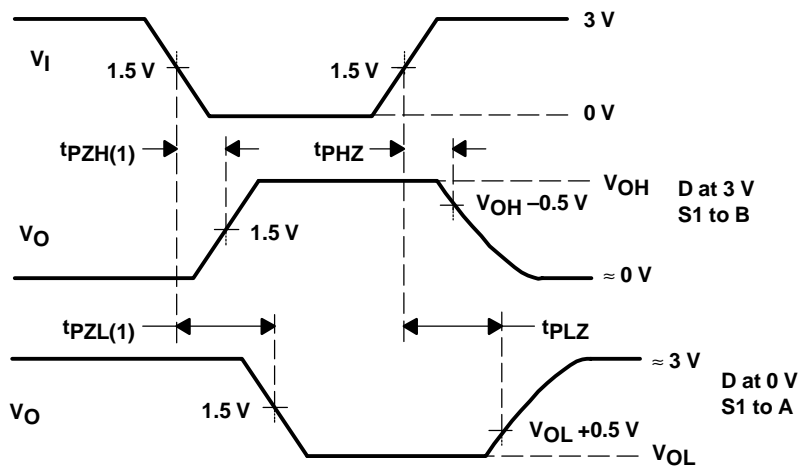


Figure 9. Receiver Enable and Disable Time Test Circuit and Voltage Waveforms With Drivers Enabled

PARAMETER MEASUREMENT INFORMATION

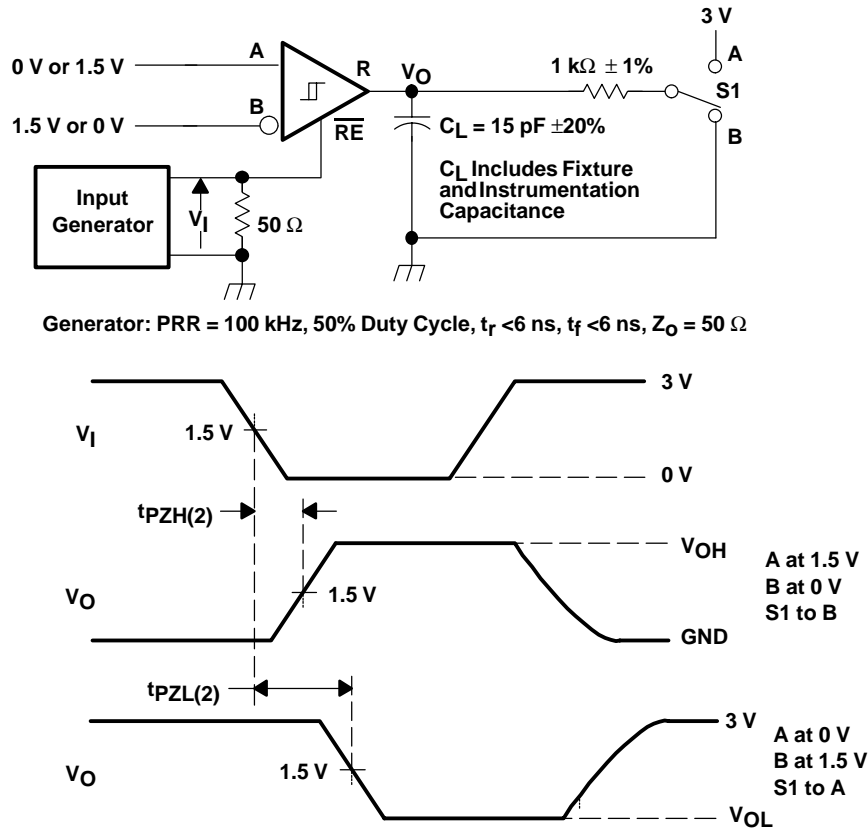
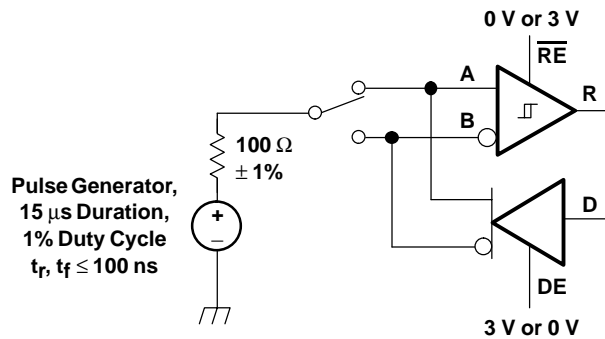


Figure 10. Receiver Enable Time From Standby (Driver Disabled)



NOTE: This test is conducted to test survivability only. Data stability at the R output is not specified.

Figure 11. Test Circuit, Transient Over Voltage Test

Function Tables

DRIVER

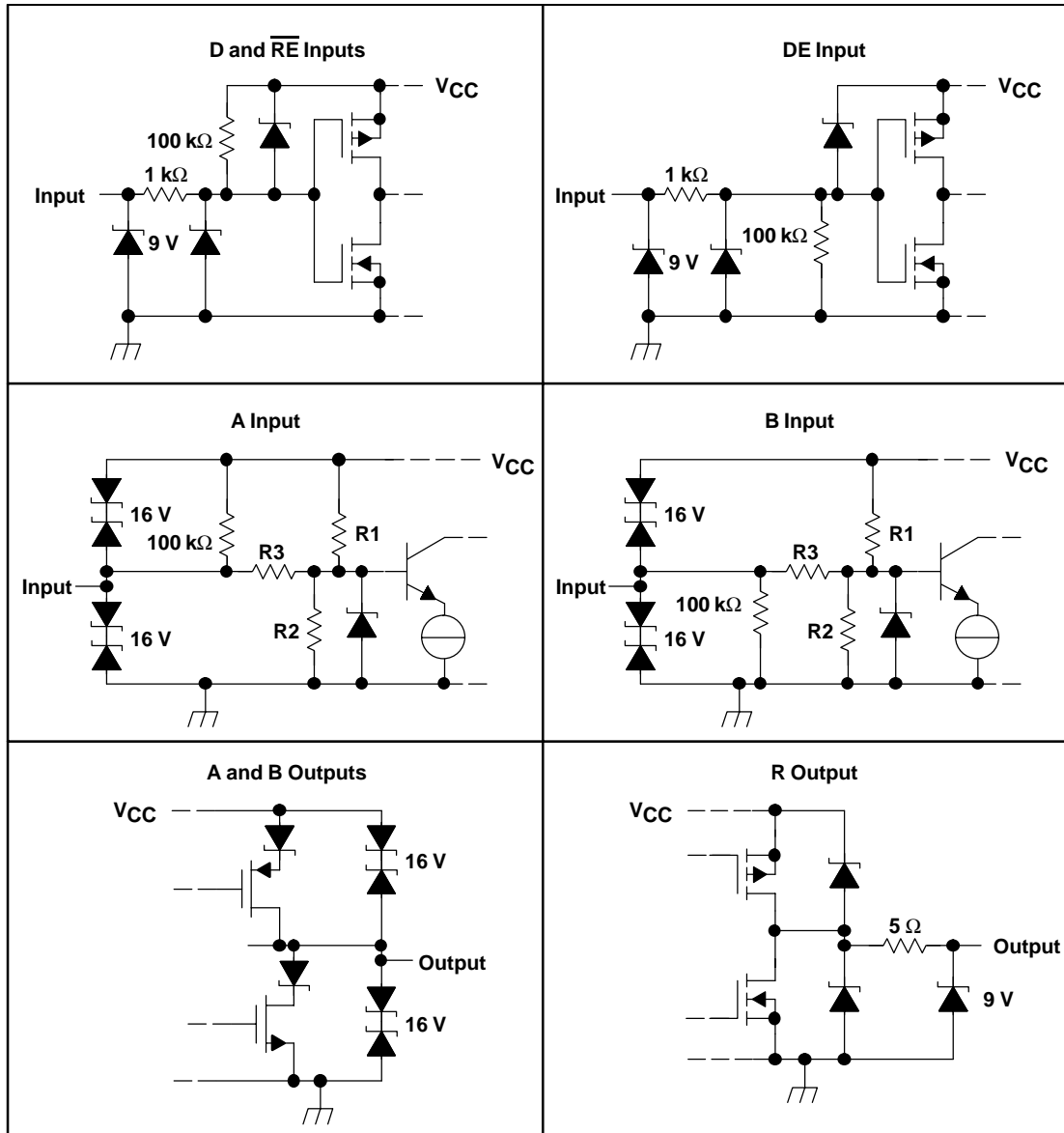
INPUT	ENABLE	OUTPUTS	
	DE	A	B
H	H	H	L
L	H	L	H
X	L	Z	Z
Open	H	H	L

RECEIVER

DIFFERENTIAL INPUTS	ENABLE	OUTPUT
$V_{ID} = V_A - V_B$	\overline{RE}	R
$V_{ID} \leq -0.2 V$	L	L
$-0.2 V < V_{ID} < -0.01 V$	L	?
$-0.01 V \leq V_{ID}$	L	H
X	H	Z
Open Circuit	L	H
Short Circuit	L	H

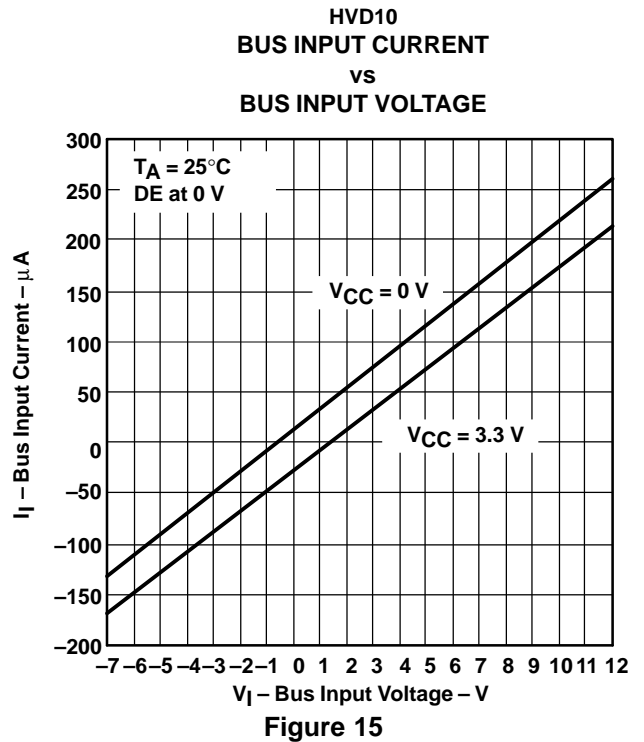
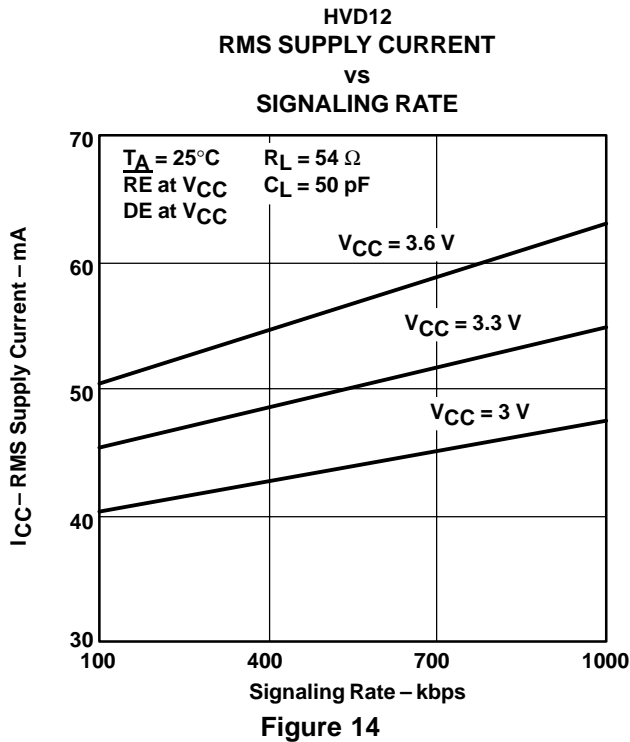
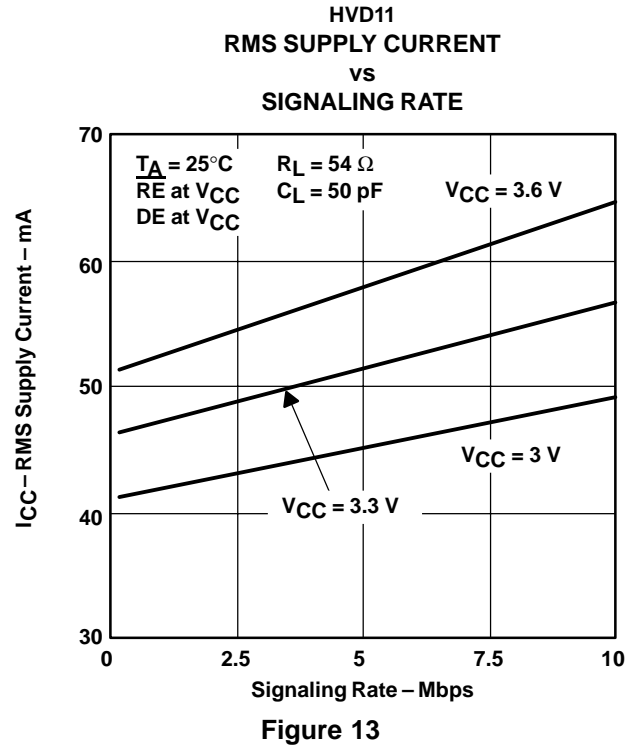
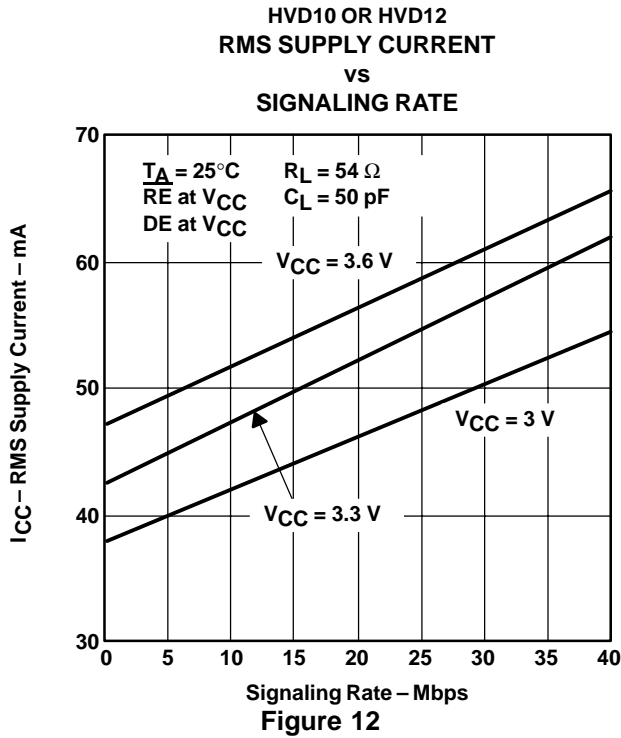
H = high level; L = low level; Z = high impedance; X = irrelevant; ? = indeterminate

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



	R1/R2	R3
SN65HVD10	9 kΩ	45 kΩ
SN65HVD11	36 kΩ	180 kΩ
SN65HVD12	36 kΩ	180 kΩ

TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS

HVD11 OR HVD12
 BUS INPUT CURRENT
 vs
 BUS INPUT VOLTAGE

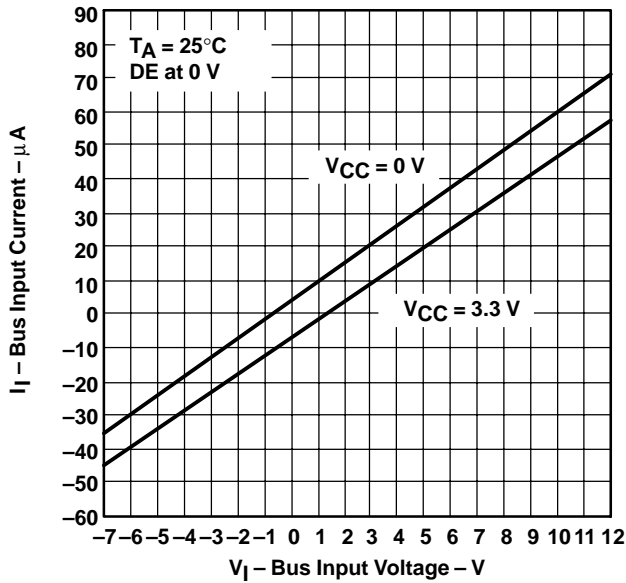


Figure 16

HIGH-LEVEL OUTPUT CURRENT
 vs
 DRIVER HIGH-LEVEL OUTPUT VOLTAGE

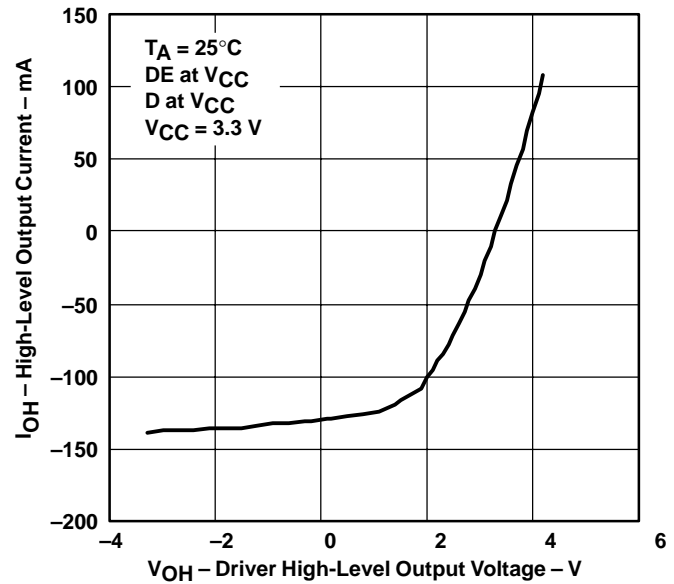


Figure 17

LOW-LEVEL OUTPUT CURRENT
 vs
 DRIVER LOW-LEVEL OUTPUT VOLTAGE

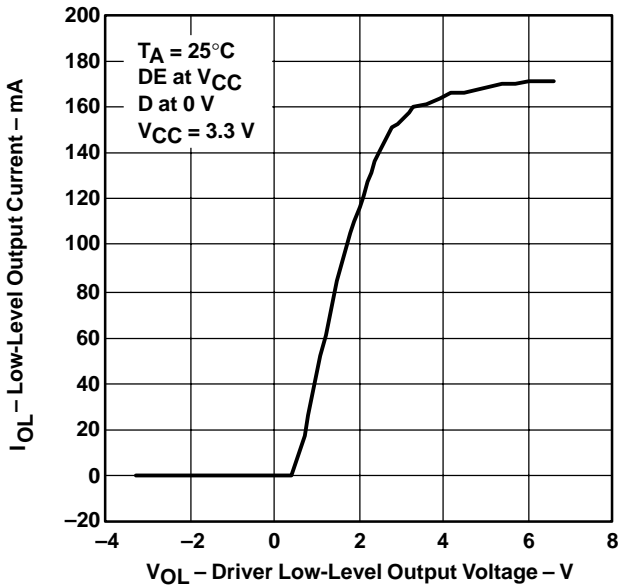


Figure 18

DRIVER DIFFERENTIAL OUTPUT
 vs
 FREE-AIR TEMPERATURE

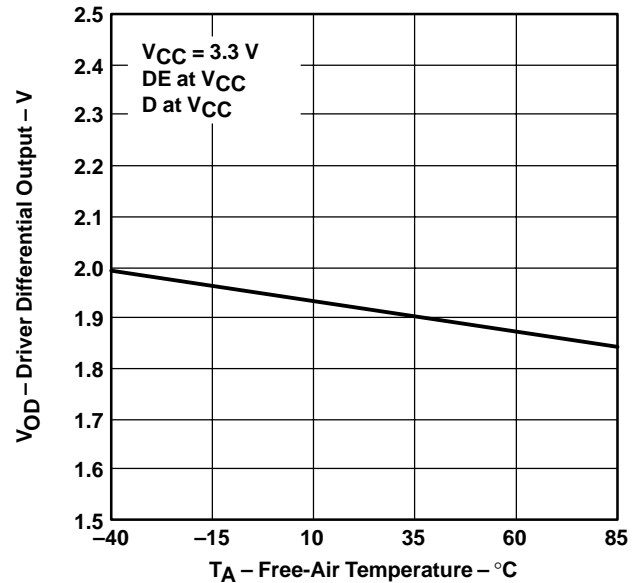


Figure 19

TYPICAL CHARACTERISTICS

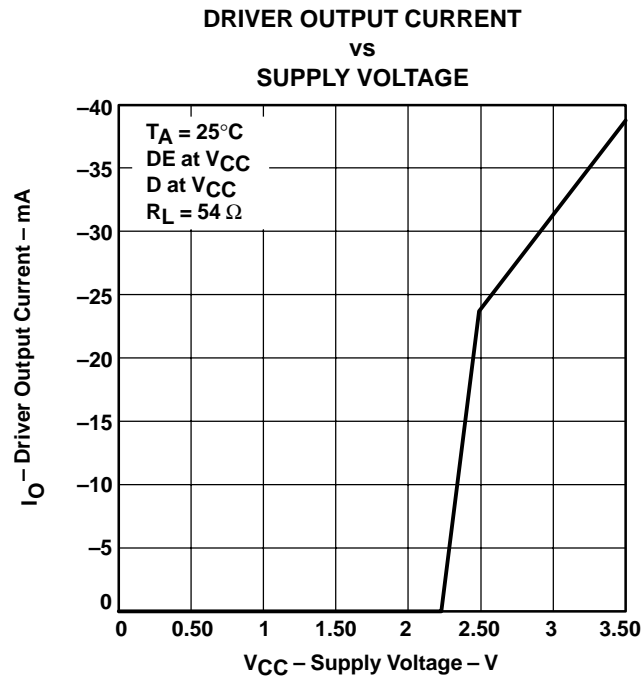
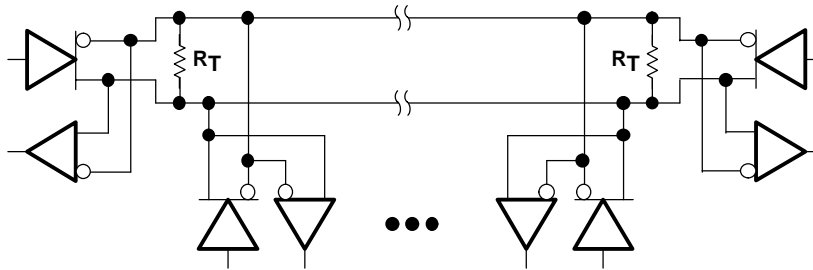


Figure 20

APPLICATION INFORMATION



Device	Number of Devices on Bus
HVD10	64
HVD11	256
HVD12	256

NOTE: The line should be terminated at both ends with its characteristic impedance ($R_T = Z_0$). Stub lengths off the main line should be kept as short as possible.

Figure 21. Typical Application Circuit

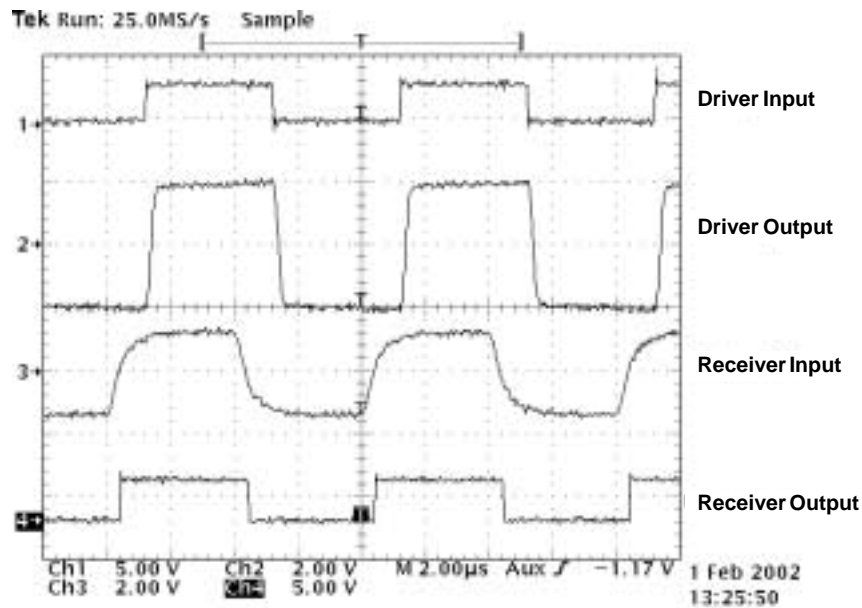


Figure 22. HVD12 Input and Output Through 2000 Feet of Cable

An example application for the HVD12 is illustrated in Figure 21. Two HVD12 transceivers are used to communicate data through a 2000 foot (600 m) length of Commscope 5524 category 5e+ twisted pair cable. The

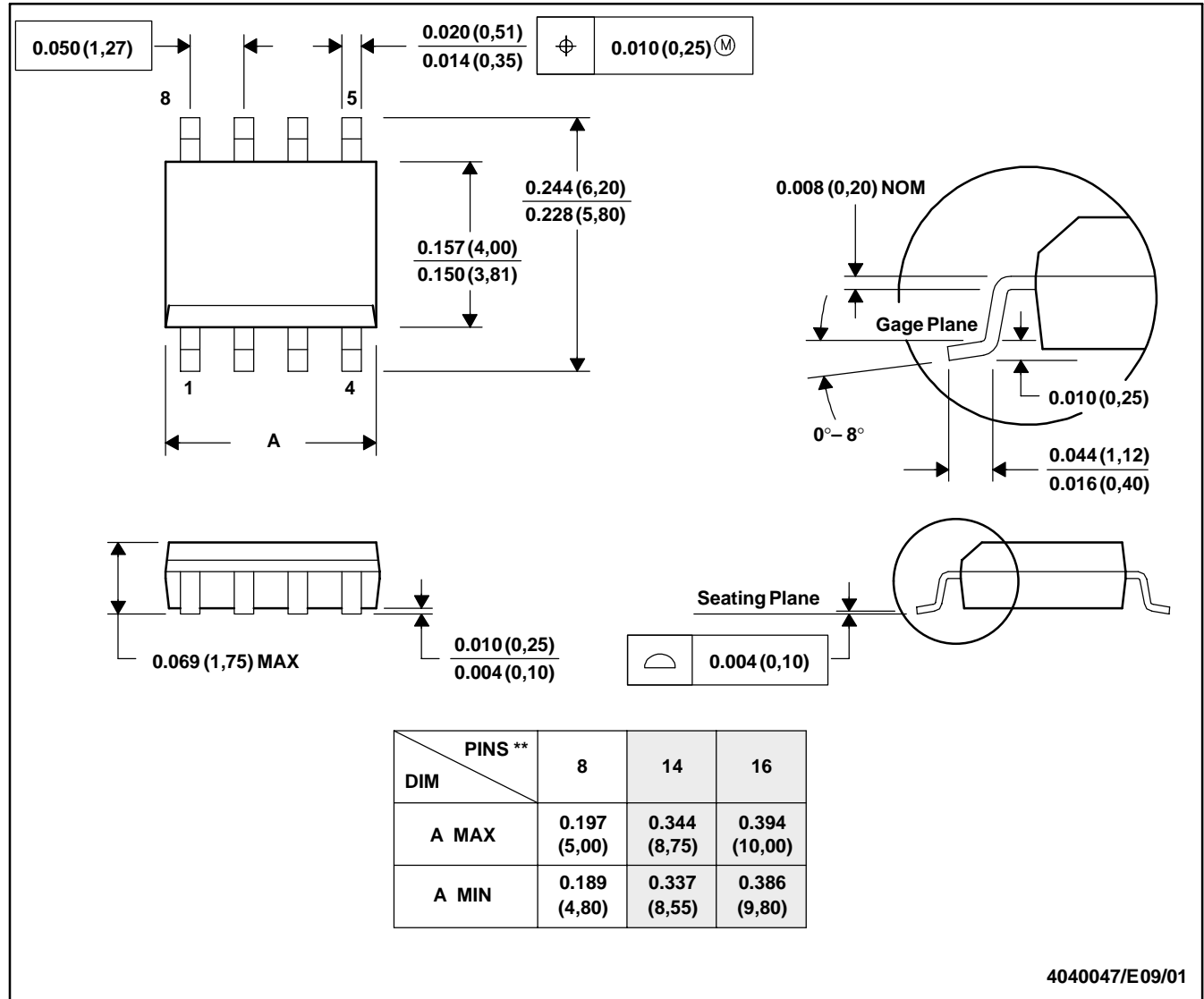
bus is terminated at each end by a 100 Ω resistor, matching the cable characteristic impedance. Figure 22 illustrates operation at a signaling rate of 250 kbps.

MECHANICAL DATA

D (R-PDSO-G**) PACKAGE

PLASTIC SMALL-OUTLINE

8 PINS SHOWN

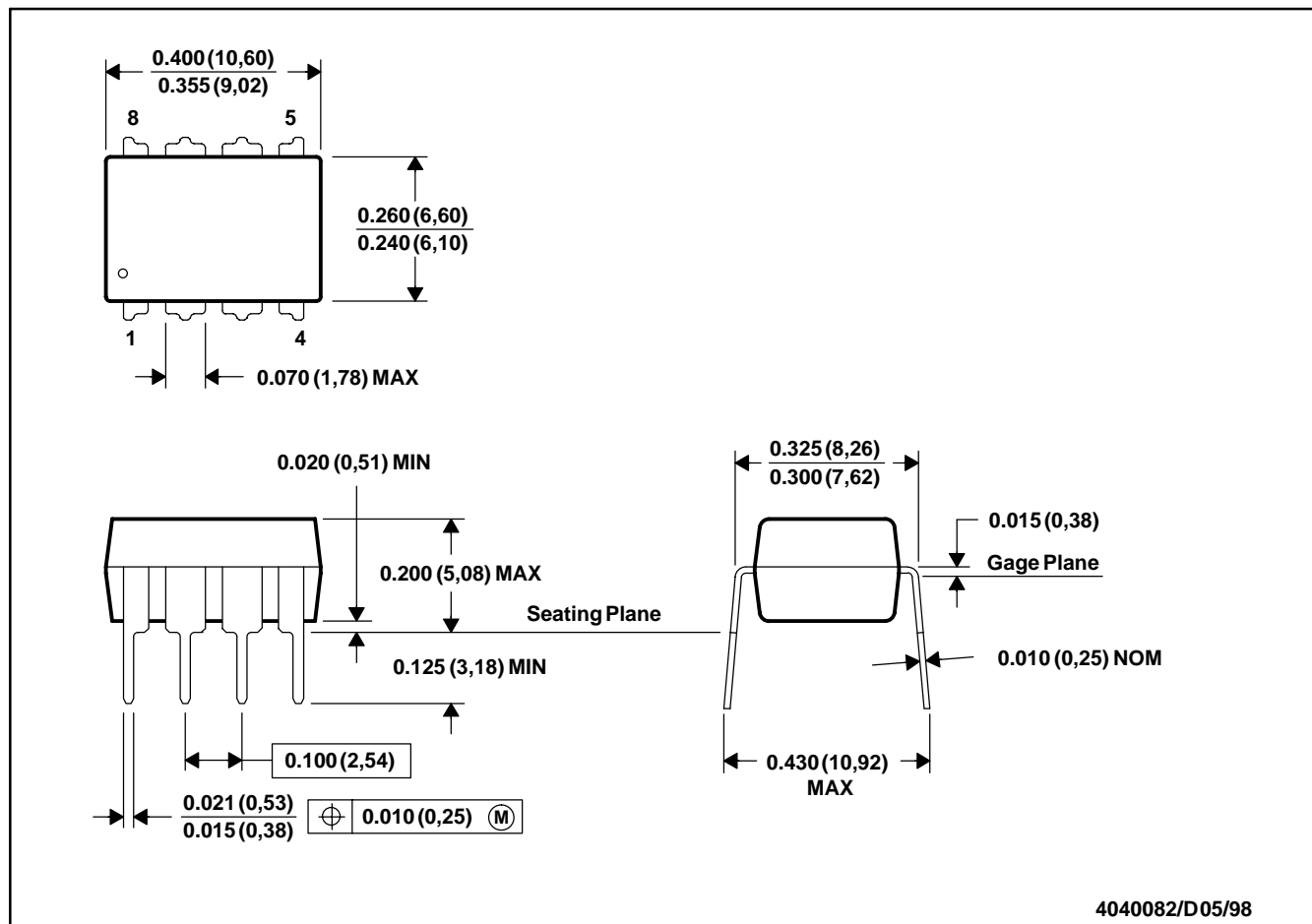


- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-012

MECHANICAL DATA

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-001

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