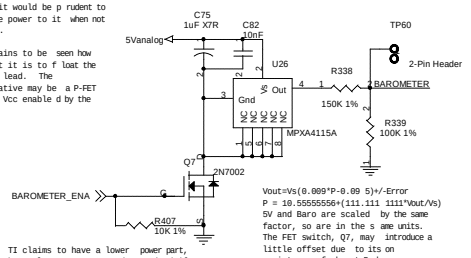
Since the sensor u ses about 60mW, it would be p rudent to disable power to it when not needed.

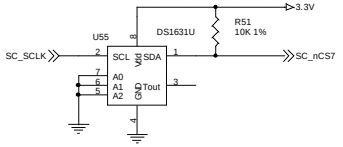
It remains to be seen how prudent it is to f loat the ground lead. The alternative may be a P-FET in the Vcc enable d by the N-FET.



TI claims to have a lower power part, but only accurate to 2 deg C (probably within the -25C and abov e range)...

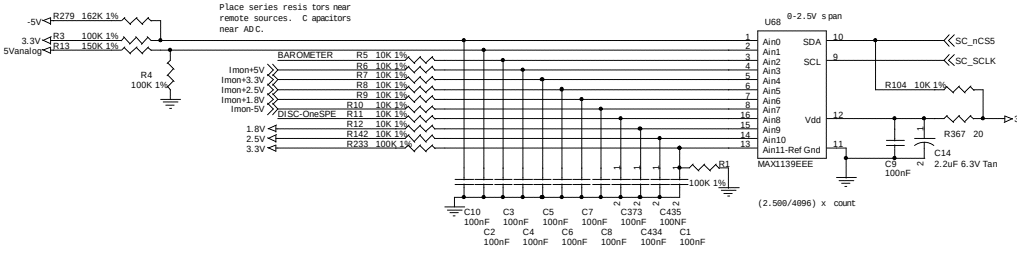
Vout=Vs(0.009*P-0.09 5)+/-Error
P = 10.55555556+(111.111 1111*Vout/Vs)
5V and Baro are scaled by the same factor, so are in the s ame units.
The FET switch, Q7, may introduce a little offset due to its on resistance of abou t 5 ohms.

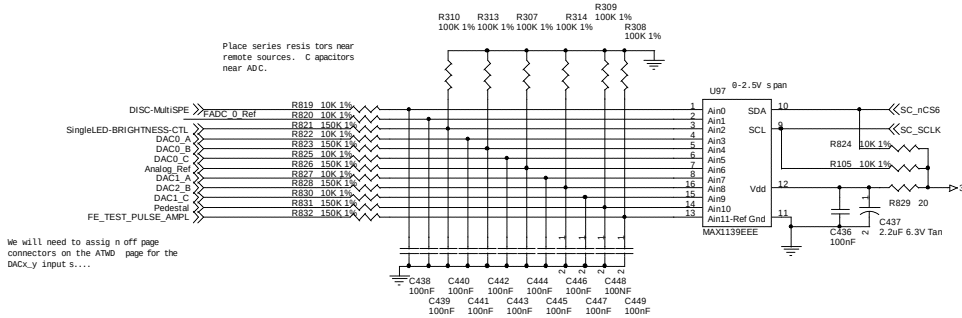
-(-5/2.5)-(+3.3+2.5+1. 8)/4 =Vout
2 - 0.825 - 0.625 - 0.4 50) = 0.100V
Lets just assume tha t if +5 is gone, we're dead. T he 5V CPU supervisory chip input will cause reboot below about 4.750V.

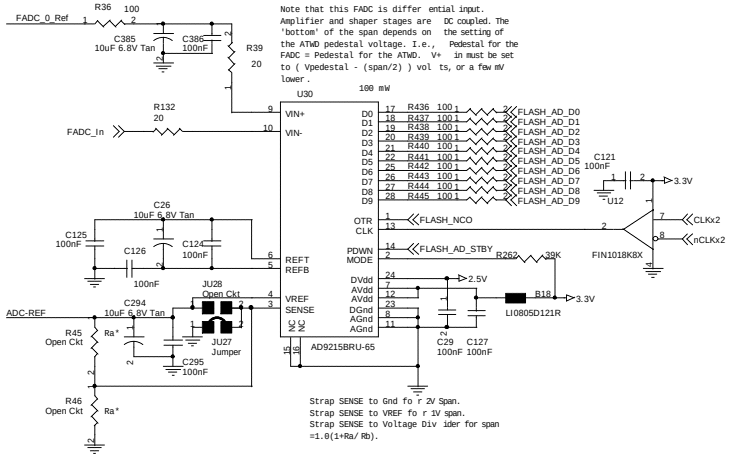


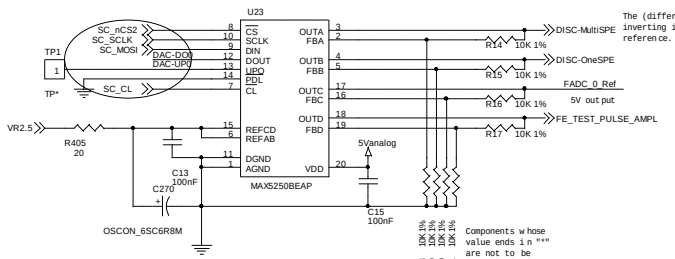
Part values ending in "*" should not be mounted. These parts are for diagnostics or implementation of alternate methodologies.

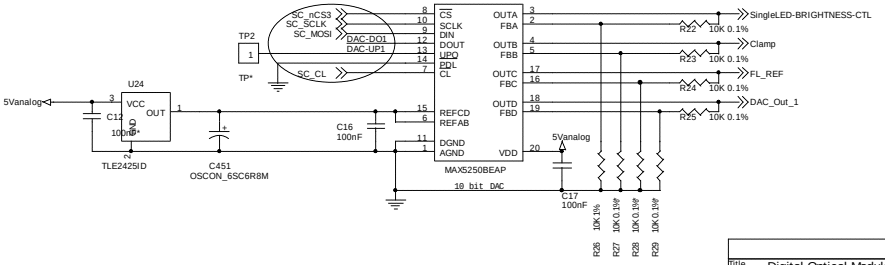
4.25 mW x 4 + 7.5mW = 24.5 mW
plus 3.3mW when converting temperature
+ 6mW x 10V/conv_ef f = 67 mW











Title	Digital Optical Module AD/DA	
Size C	Document Number <Doc>	Rev 1.1
Date: Friday, May 16, 2003	Sheet 4 of 15	

Nov 25, '02 GTP
Name change to
eliminate
naming conflict

Per criterion established July 2002 (gtp&drn) the design goal for the IceCube DOM is 200 PE = 1V into the ATWD dic tated by PMT saturation behavior. Namely, the PMT NEVER delivers mor e than about 2V, and is linear to about 1V into a 50 ohm load (100 oh m || back-termination).

Caution: The comparato rs are 5V parts that cannot be op erated from 3.3V. Care must be take n to protect the driven 3.3 V part.

Locate these amplifiers --> close to the PMT signal input.

1*1.3*5 + 2*1.3*5 + 6.8*10 + 2* 1.15*10+2*1.1*5+ 3*0.4*10=13 4 mW
opamp comparator, 1135 80 14 8014 8005

AD advertises that these (400 MHz) amplifiers re cover in 60 ns. At 5 mW per stage, they give slightly less performance than an HA1135 at 1/10th the current. Saturation is not a big issue for t he (latching) comparator input, since latch recovery is contr olled by the FPGA

If we have power to burn, once all revisions are taken into account, the 850 MHz bandwidth HA1135 may prove to be a bett er choice as comparator input amplifier, as one stage should hav e less delay than 2.

The comparators exhibit less trigger delay i f driven by a positive signal, so the second gain stage inverts. The first one buffers to minimize load on the PMT signal.

If test pulser, U52, injects too much power supply noise, it will have to go, in favor of something that is quieter.

Calibration input test-point. Drive with 5V square wave to generate fixed amplitude test pulses.

SamTec SMM-102 -01-S-D Thru-Hole 2x2 2m m socket mates with S amTec TW-02-01-S-D-120-08 0 2x2 2mm break-away h eader

optimized for 200 MHz BW Also try observi ng the performance of this stage with 499 a nd 249 ohm feedback div ider. See if it is st ill as stable. It shoul d have more bandwi dth.

Test pulse inj ection (if it doesn't work, remove transf ormer, and use jum per.)

If the PMT delivers 3V into a 50 ohm load, then change the divider resistors to R30=31.6 a nd R54=63.4 Leave the gain of the amplifier unchanged. The design goal is to have the PMT saturation volta ge within the span of the ATWD.

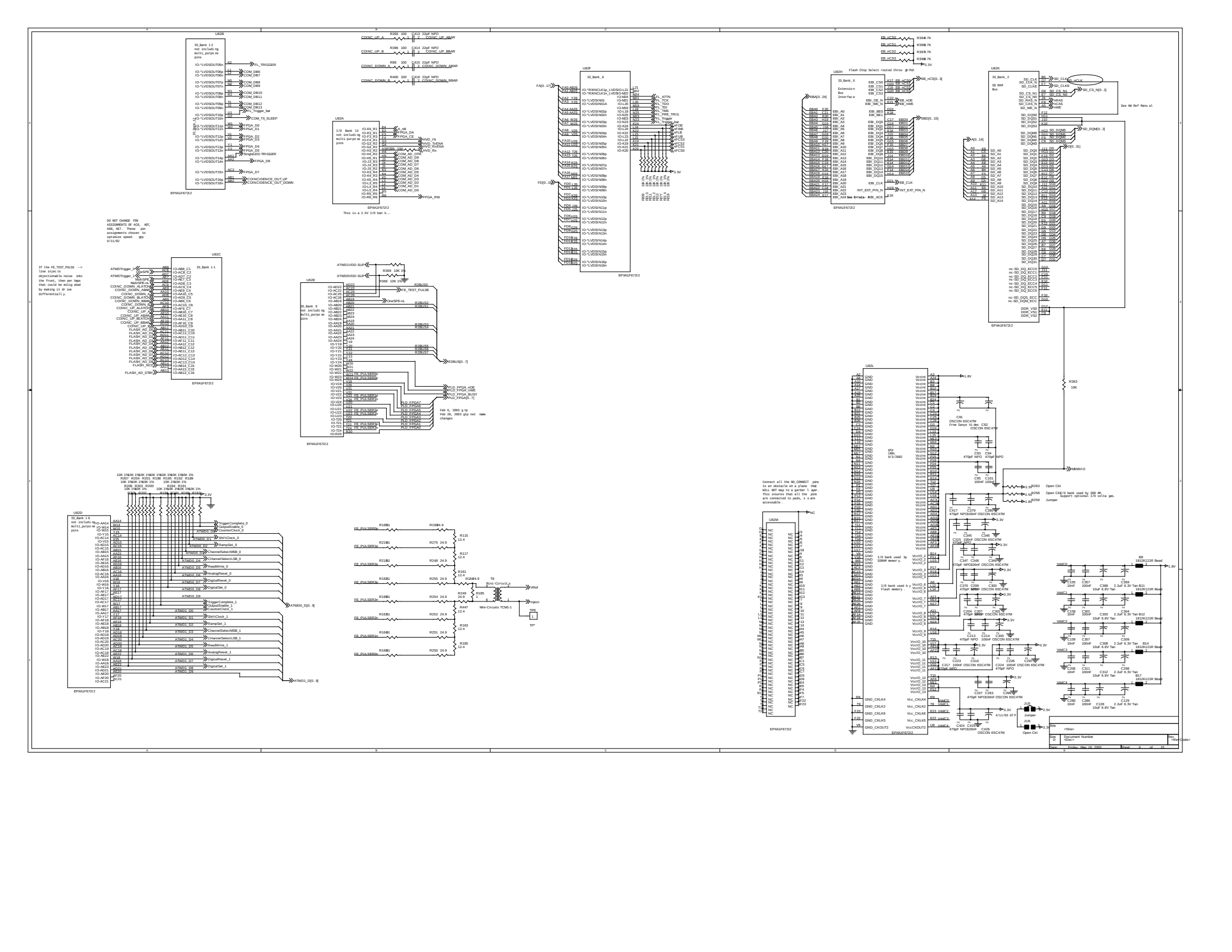
Distribute capacitors around th e island of Vref. If some are not needed, they ma y not be mounted.

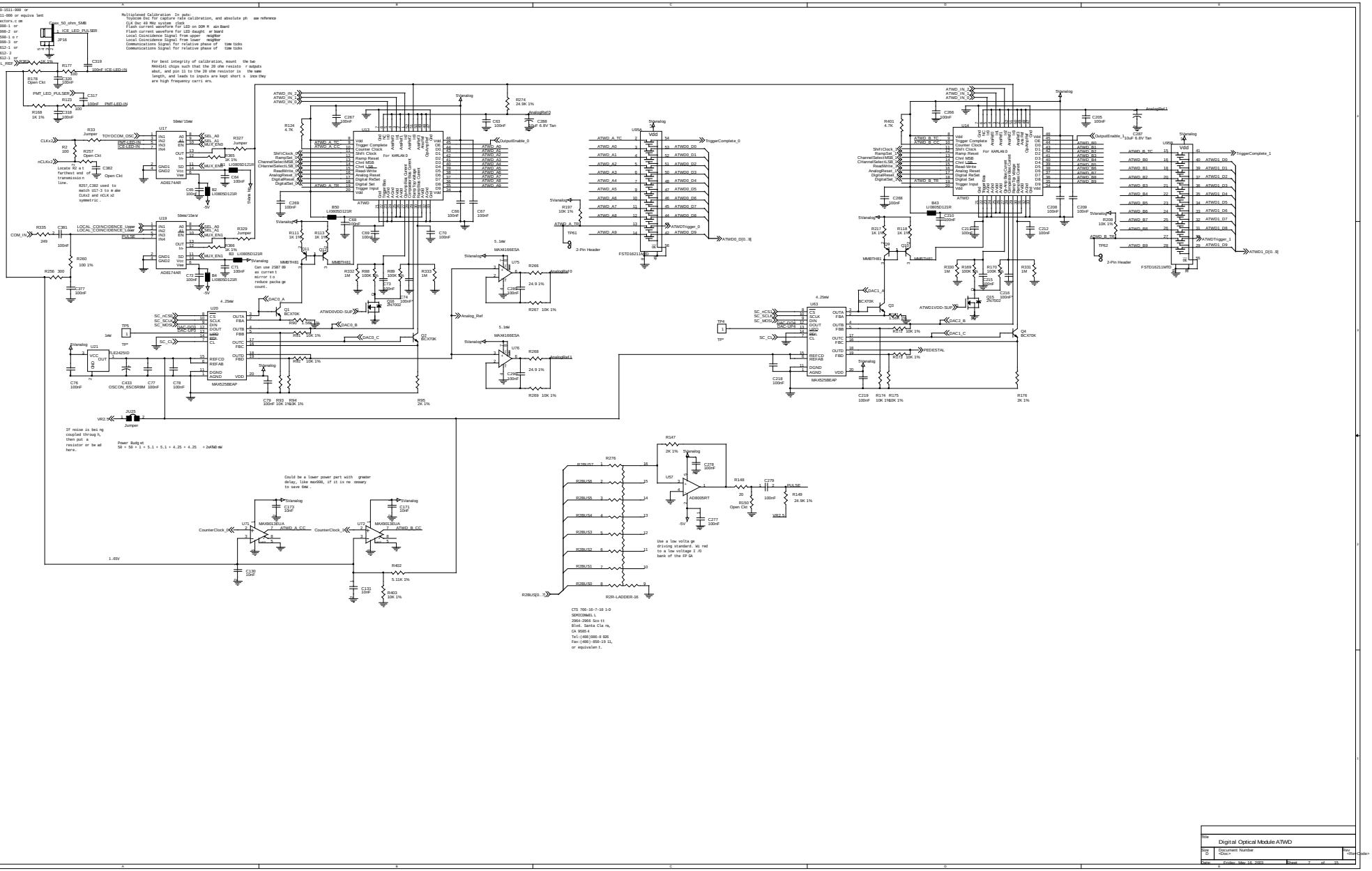
The shaped signal path design was from Harold Yaver of the Engineering Department.
-Modifications added to insure stable off set behavior, and to off set the output to match the input range of the ADC

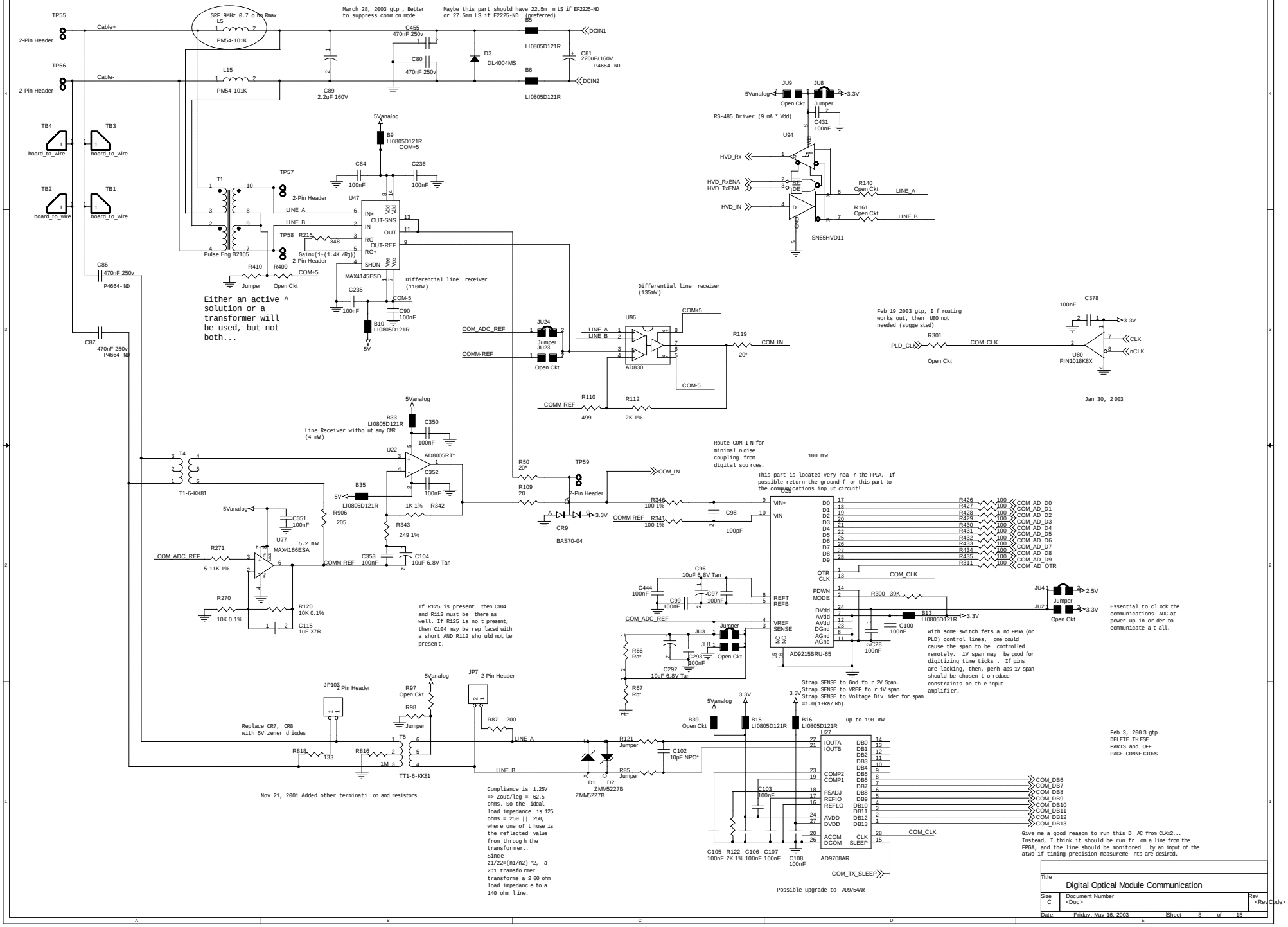
Jan 19, 2003 Correct reversed polarized capacitors on analog stages. gtp

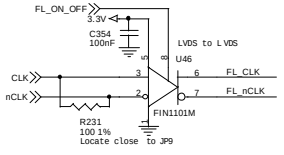
to... Martin Keste l 3/30/03

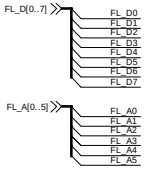
Lawrence Berkeley National Laboratory		GTP/JL/DRN/HY
Title: Digital Optical Module Analog Front End		
Size: C	Document Number: <Doc>	Rev: 0
Date: Friday, May 16, 2003	Sheet 5 of 15	

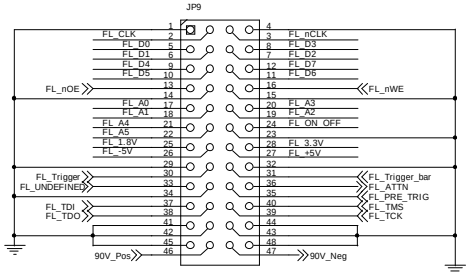



Digital Optical Module ATWD
Size: D
Document Number: <Doc>
Rev: <RevCode>
Date: Friday, May 16, 2003
Sheet 7 of 15


March 28, 2003 gtp , Better to suppress comm on mode
Maybe this part should have 22.5m m LS if EF2225-ND or 27.5mm LS if E2225-ND (preferred)
TP55
Cable+
2-Pin Header
SRF 9MHz 0.7 o hm Rmax
L5
PM54-101K
C455
470nF 250v
C80
470nF 250v
D3
DL4004MS
B5
LI0805D121R
DCIN1
C81
220uF/160V
P4664-ND
TP56
Cable-
2-Pin Header
L15
PM54-101K
C89
2.2uF 160V
B6
LI0805D121R
DCIN2
TB4
board_to_wire
TB3
board_to_wire
TB2
board_to_wire
TB1
board_to_wire
T1
Pulse Eng B2105
TP57
2-Pin Header
TP58
2-Pin Header
R215
348
Gain=(1+(1.4K /Rg))
LINE_A
LINE_B
U47
MAX4145ESD
IN+
IN-
RG-
RG+
SHDN
OUT-SNS
OUT
OUT-REF
Differential line receiver (110mW)
5Vanalog
B9
LI0805D121R
COM+5
C84
100nF
C236
100nF
C235
100nF
C90
100nF
COM-5
B10
LI0805D121R
-5V
R410
Jumper
R409
Open Ckt
COM+5
C86
470nF 250v
P4664-ND
C87
470nF 250v
P4664-ND
Either an active ^ solution or a transformer will be used, but not both...
Differential line receiver (135mW)
COM_ADC_REF
COMM-REF
JU24
Jumper
JU23
Open Ckt
U96
AD830
LINE_A
LINE_B
COM+5
COM-5
R119
20*
COM_IN
R110
499
R112
2K 1%
COMM-REF
Feb 19 2003 gtp, I f routing works out, then U80 not needed (sugge sted)
PLD_CLK
R301
Open Ckt
COM_CLK
C378
100nF
3.3V
CLK
nCLK
U80
FIN1018K8X
Jan 30, 2003
RS-485 Driver (9 mA * Vdd)
JU9
5Vanalog
Open Ckt
JU8
3.3V
Jumper
C431
100nF
U94
HVD_Rx
HVD_RxENA
HVD_TxENA
HVD_IN
R140
Open Ckt
LINE_A
R161
Open Ckt
LINE_B
SN65HVD11
Line Receiver witho ut any CMR (4 mW)
B33
LI0805D121R
5Vanalog
C350
100nF
U22
AD8005RT*
C352
100nF
T4
T1-6-KK81
B35
-5V
LI0805D121R
1K 1%
R342
R343
249 1%
C104
10uF 6.8V Tan
C353
100nF
R906
205
5Vanalog
C351
100nF
U77
MAX4166ESA
5.2 mW
R271
5.11K 1%
COM_ADC_REF
COMM-REF
R270
10K 0.1%
R120
10K 0.1%
C115
1uF X7R
If R125 is present then C104 and R112 must be there as well. If R125 is no t present, then C104 may be rep laced with a short AND R112 sho uld not be present.
R50
20*
R109
20
TP59
2-Pin Header
COM_IN
Route COM I N for minimal n oise coupling fr om digital sou rces.
100 mW
This part is located very nea r the FPGA. If possible return the ground f or this part to the communications inp ut circuit!
R346
100 1%
R341
100 1%
C98
100pF
CR9
BAS70-04
3.3V
U25
AD9215BRU-65
VIN+
VIN-
REFT
REFB
VREF
SENSE
OTR
CLK
PDWN
MODE
DVdd
AVdd
AVdd
DGnd
AGnd
AGnd
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
R426
R427
R428
R429
R430
R431
R432
R433
R434
R435
R311
COM_AD_D0
COM_AD_D1
COM_AD_D2
COM_AD_D3
COM_AD_D4
COM_AD_D5
COM_AD_D6
COM_AD_D7
COM_AD_D8
COM_AD_D9
COM_AD_OTR
COM_CLK
C96
10uF 6.8V Tan
C444
100nF
C99
100nF
C97
100nF
R300
39K
JU4
Jumper
JU2
Open Ckt
2.5V
3.3V
Essential to cl ock the communications ADC at power up in or der to communicate a t all.
B13
LI0805D121R
3.3V
C100
100nF
C28
100nF
With some switch fets a nd FPGA (or PLD) control lines, one could cause the span to be controlled remotely. 1V span may be good for digitizing time ticks . If pins are lacking, then, perh aps 1V span should be chosen t o reduce constraints on th e input amplifier.
JU3
Jumper
JU1
Open Ckt
C293
100nF
C292
10uF 6.8V Tan
R66
Ra*
R67
Rb*
Strap SENSE to Gnd fo r 2V Span.
Strap SENSE to VREF fo r 1V span.
Strap SENSE to Voltage Div ider for span =1.0(1+Ra/ Rb).
JP103
2 Pin Header
JP7
2 Pin Header
R97
Open Ckt
R98
Jumper
R87
200
Replace CR7, CR8 with 5V zener d iodes
R818
133
R816
1M 3
TT1-6-KK81
LINE_A
LINE_B
R121
Jumper
R85
Jumper
C102
10pF NPO*
D1
D2
ZMM5227B
ZMM5227B
Compliance is 1.25V => Zout/leg = 62.5 ohms. So the ideal load impedance is 125 ohms = 250 || 250, where one of t hose is the reflected value from throug h the transform er.. Since z1/z2=(n1/n2) ^2, a 2:1 transfo rmer transforms a 2 00 ohm load impedanc e to a 140 ohm l ine.
Nov 21, 2001 Added other terminati on and resistors
B39
Open Ckt
B15
LI0805D121R
B16
LI0805D121R
up to 190 mW
U27
AD9708AR
IOUTA
IOUTB
COMP2
COMP1
FSADJ
REFIO
REFLO
AVDD
DVDD
ACOM
DCOM
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
DB8
DB9
DB10
DB11
DB12
DB13
CLK
SLEEP
C103
100nF
C105
100nF
R122
2K 1%
C106
100nF
C107
100nF
C108
100nF
COM_CLK
COM_TX_SLEEP
COM_DB6
COM_DB7
COM_DB8
COM_DB9
COM_DB10
COM_DB11
COM_DB12
COM_DB13
Possible upgrade to AD9754AR
Feb 3, 2003 gtp DELETE TH ESE PARTS and OFF PAGE CONNE CTORS
Give me a good reason to run this D AC from CLKx2... Instead, I think it should be run fr om a line from the FPGA, and the line should be monitored by an input of the atwd if timing precision measureme nts are desired.
Title
Digital Optical Module Communication
Size C
Document Number <Doc>
Rev <Rev Code>
Date: Friday, May 16, 2003
Sheet 8 of 15







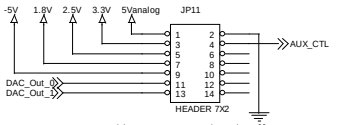
12 x 4 SamTec ESQT-112-02-L-Q-078

Looking down on the comp onent side of the DOM main PCB the pin pattern will look like the ima ge above

1	GND
2	CLK
3	C LK\
4	GND
5	F L_D0
6	F L_D1
7	F L_D2
8	F L_D3
9	F L_D4
10	F L_D5
11	F L_D6
12	F L_D7
13	RD\
14	GND
15	GND
16	WR\
17	F L_A0
18	F L_A1
19	F L_A2
20	F L_A3
21	F L_A4
22	F L_A5
23	GND
24	ON /OFF
25	1 .8V
26	+5V
27	-5V
28	3 .3V
29	GND
30	T RIG
31	T RIG\
32	GND
33	Unde fined
34	GND
35	PRE _TRIG
36	FL_ ATTN
37	TDI
38	TDO
39	TCK
40	TMS
41	GND
42	GND
43	GND
44	GND
45	GND
46	90V _Pos
47	90V _Neg
48	GND
45	GND

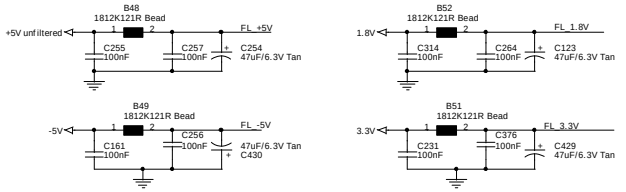
In the 4x10 arrangement, this looks l ike the following:

GND	FL_D0	FL_D4	RD\	FL_A0	FL_A4	1.8V	GND	Undef	TDI	GND	GND
CLK	FL_D1	FL_D5	GND	FL_A1	FL_A5	+5V	TRIG	GND	TDO	GND	90V Pos
CLK\	FL_D2	FL_D6	GND	FL_A2	GND	-5V	TRIG\	PRE_TRIG	TCK	GND	90V_Neg
GND	FL_D3	FL_D7	WR\	FL_A3	ON/OFF	3.3V	GND	ATTN	TMS	GND	GND

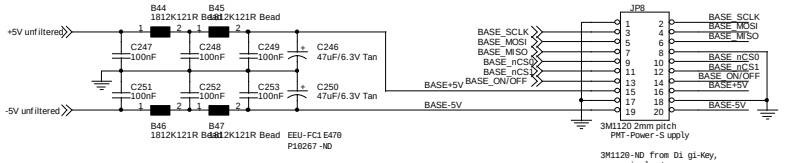


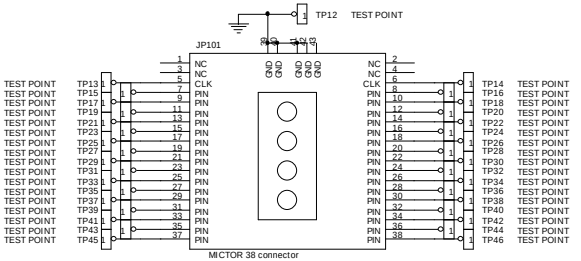
Mount this connector anyw here that all power supply voltages ar e available.

Can be used to power and control altern ate PMT power supply



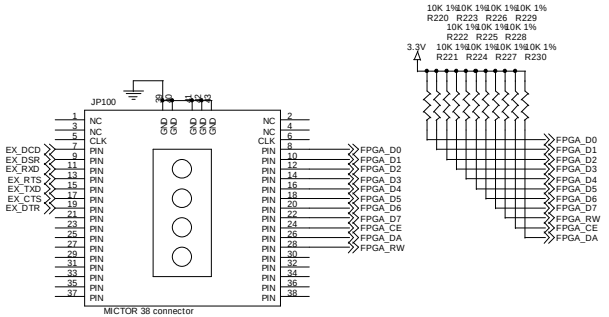
1 GND
2 SCK - Serial clock
3 SCK
4 MOSI -Serial data in
5 MOSI
6 MISO - Serial d ata out
7 MISO
8 GND
9 CS0 (DAC) - Chip sele ct for DAC
10 CS0
11 CS1 (ADC) - Chip sel ect for ADC
12 CS1
13 ON/OFF - Power supply e nable/disable
14 ON/OFF
15 +5V - Main power
16 +5V
17 GND
18 GND
19 -5V - Main power
20 -5V
to match the interface do cument, Jan 02, '03





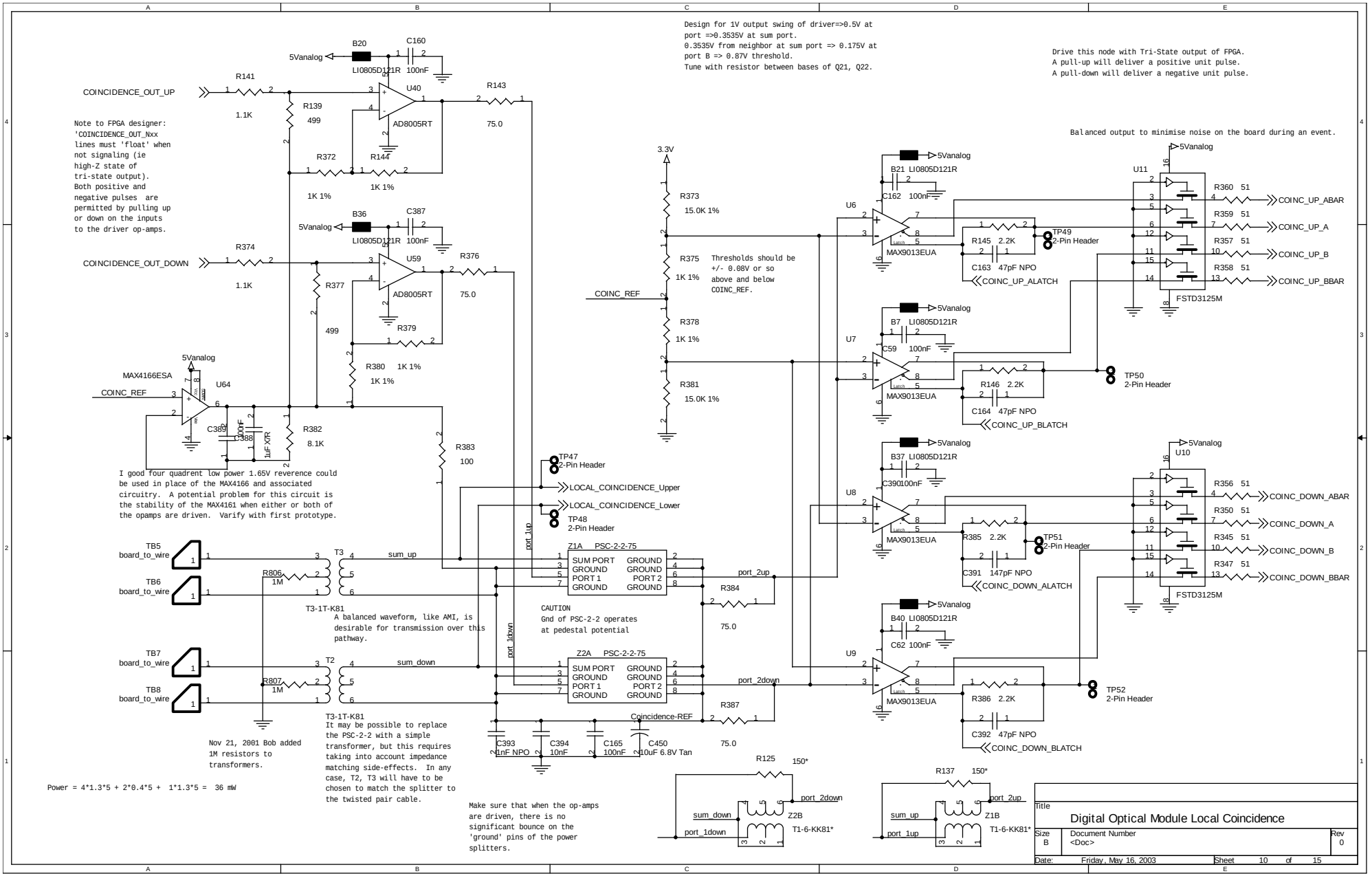
This connector is meant to be used dur ing pre-production debugging. The footpring should be mounted on a part of the board that is later broken off and discarded. T he test-points will be used to tack down one of wires that bring s ignals out of the main board.

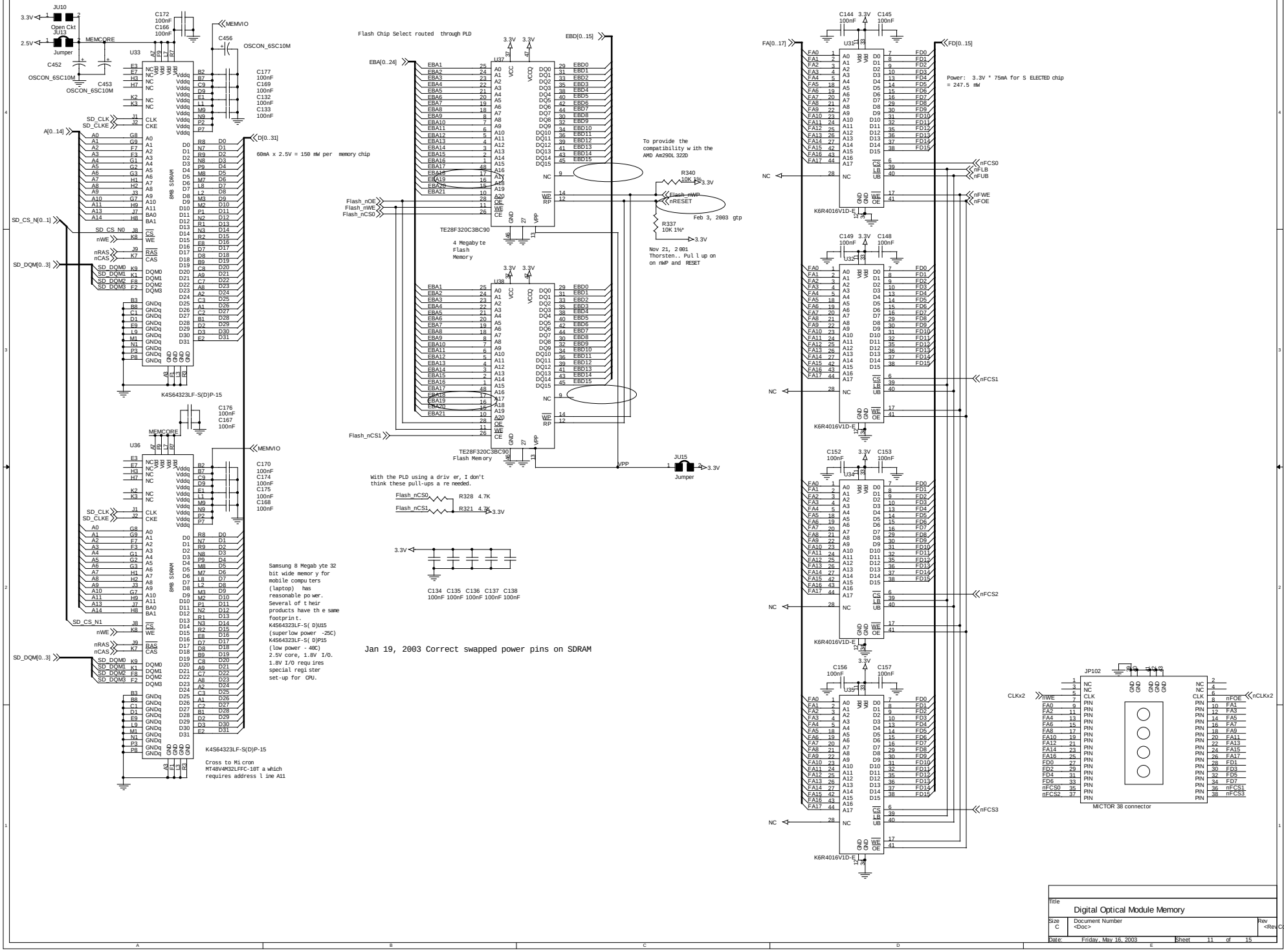
Compatible with model P6434 probe for Tektronix logic analyzer.



Compatible with model P6434 probe for Tektronix logic analyzer.

Title	Off-Board Subsystems	
Size C	Document Number <Doc>	Rev <Rev Code>
Date: Friday, May 16, 2003	Sheet 9 of 15	


Design for 1V output swing of driver=>0.5V at port =>0.3535V at sum port.
0.3535V from neighbor at sum port => 0.175V at port B => 0.87V threshold.
Tune with resistor between bases of Q21, Q22.
Drive this node with Tri-State output of FPGA.
A pull-up will deliver a positive unit pulse.
A pull-down will deliver a negative unit pulse.
Balanced output to minimise noise on the board during an event.
COINCIDENCE_OUT_UP
COINCIDENCE_OUT_DOWN
Note to FPGA designer:
'COINCIDENCE_OUT_Nxx lines must 'float' when not signaling (ie high-Z state of tri-state output).
Both positive and negative pulses are permitted by pulling up or down on the inputs to the driver op-amps.
5Vanalog
LI0805D121R
AD8005RT
MAX4166ESA
COINC_REF
3.3V
Thresholds should be +/- 0.08V or so above and below COINC_REF.
MAX9013EUA
FSTD3125M
COINC_UP_ABAR
COINC_UP_A
COINC_UP_B
COINC_UP_BBAR
COINC_UP_ALATCH
COINC_UP_BLATCH
COINC_DOWN_ABAR
COINC_DOWN_A
COINC_DOWN_B
COINC_DOWN_BBAR
COINC_DOWN_ALATCH
COINC_DOWN_BLATCH
I good four quadrent low power 1.65V reverence could be used in place of the MAX4166 and associated circuitry. A potential problem for this circuit is the stability of the MAX4161 when either or both of the opamps are driven. Varify with first prototype.
LOCAL_COINCIDENCE_Upper
LOCAL_COINCIDENCE_Lower
TP47 2-Pin Header
TP48 2-Pin Header
TP49 2-Pin Header
TP50 2-Pin Header
TP51 2-Pin Header
TP52 2-Pin Header
TB5 board_to_wire
TB6 board_to_wire
TB7 board_to_wire
TB8 board_to_wire
T3-1T-K81
A balanced waveform, like AMI, is desirable for transmission over this pathway.
CAUTION
Gnd of PSC-2-2 operates at pedestal potential
Z1A PSC-2-2-75
Z2A PSC-2-2-75
SUM PORT
GROUND
PORT 1
PORT 2
sum_up
sum_down
port_1up
port_1down
port_2up
port_2down
Coincidence-REF
Nov 21, 2001 Bob added 1M resistors to transformers.
It may be possible to replace the PSC-2-2 with a simple transformer, but this requires taking into account impedance matching side-effects. In any case, T2, T3 will have to be chosen to match the splitter to the twisted pair cable.
Make sure that when the op-amps are driven, there is no significant bounce on the 'ground' pins of the power splitters.
Power = 4*1.3*5 + 2*0.4*5 + 1*1.3*5 = 36 mW
T1-6-KK81*
Z1B
Z2B
Title
Digital Optical Module Local Coincidence
Size B
Document Number <Doc>
Rev 0
Date: Friday, May 16, 2003
Sheet 10 of 15


JU10
Open Ckt
JU13
Jumper
MEMCORE
MEMVIO
OSCON_6SC10M
C452
C453
C172 100nF
C166 100nF
C456
C177 100nF
C169 100nF
C132 100nF
C133 100nF
U33
SD_CLK
SD_CLKE
A[0..14]
D[0..31]
60mA x 2.5V = 150 mW per memory chip
SD_CS_N[0..1]
SD_CS N0
nWE
nRAS
nCAS
SD_DQM[0..3]
8MB S90AM
K4S64323LF-S(D)P-15
C176 100nF
C167 100nF
U36
C170 100nF
C174 100nF
C175 100nF
C168 100nF
SD_CS_N1
Samsung 8 Megab yte 32 bit wide memor y for mobile comput ers (laptop) has reasonable po wer. Several of t heir products have th e same footprint. K4S64323LF-S(D)U15 (superlow power -25C) K4S64323LF-S(D)P15 (low power - 40C) 2.5V core, 1.8V I/O. 1.8V I/O requ ires special regi ster set-up for CPU.
Cross to Mi cron MT48V4M32LFFC-10T a which requires address l ine A11
Flash Chip Select routed through PLD
EBA[0..24]
EBD[0..15]
U37
U38
TE28F320C3BC90
4 Megabyte Flash Memory
Flash_nOE
Flash_nWE
Flash_nCS0
Flash_nCS1
To provide the compatibility w ith the AMD Am29DL 322D
R340 10K 1%
R337 10K 1%*
Flash_nWP
nRESET
Feb 3, 2003 gtp
Nov 21, 2001 Thorsten.. Pul l up on on nWP and RESET
JU15
Jumper
VPP
With the PLD using a driv er, I don't think these pull-ups a re needed.
R328 4.7K
R321 4.7K
C134 100nF
C135 100nF
C136 100nF
C137 100nF
C138 100nF
Jan 19, 2003 Correct swapped power pins on SDRAM
FA[0..17]
FD[0..15]
U31
U32
U34
U35
C144 100nF
C145 100nF
C149 100nF
C148 100nF
C152 100nF
C153 100nF
C156 100nF
C157 100nF
K6R4016V1D-E
nFCS0
nFLB
nFUB
nFWE
nFOE
nFCS1
nFCS2
nFCS3
Power: 3.3V * 75mA for S ELECTED chip = 247.5 mW
JP102
CLKx2
nCLKx2
MICTOR 38 connector
Title
Digital Optical Module Memory
Size C
Document Number <Doc>
Rev <Rev Code>
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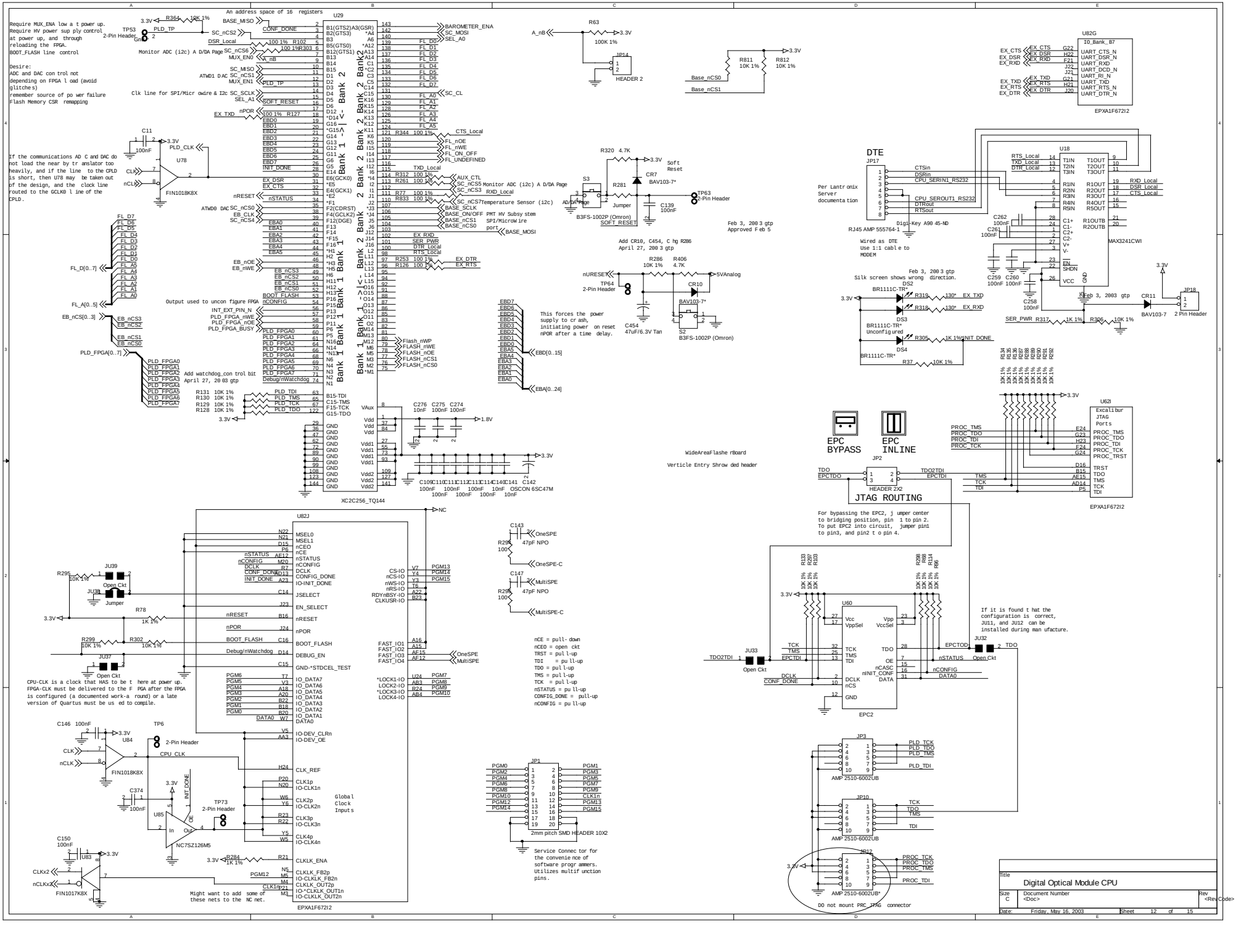
An address space of 16 registers
Require MUX_ENA low a t power up.
Require HV power sup ply control at power up, and through reloading the FPGA.
BOOT_FLASH line control
Desire:
ADC and DAC con trol not depending on FPGA l oad (avoid glitche s)
remember source of po wer failure
Flash Memory CSR remapping
Monitor ADC (i2c) A D/DA Page
Clk line for SPI/Micr owire & I2c SC_SCLK
If the communications AD C and DAC do not load the near by tr anslator too heavily, and if the line to the CPLD is short, then U78 may be taken out of the design, and the clock line routed to the GCLK0 l ine of the CPLD.
Output used to uncon figure FPGA
Add watchdog_con trol bit April 27, 20 03 gtp
Monitor ADC (i2c) A D/DA Page
Temperature Sensor (i2c)
PMT HV Subsy stem SPI/Microw ire port
Add CR10, C454, C hg R286 April 27, 200 3 gtp
This forces the power supply to cr ash, initiating power on reset nPOR after a time delay.
Feb 3, 200 3 gtp Approved F eb 5
Feb 3, 200 3 gtp
Silk screen shows wrong direction.
Per Lantr onix Server documenta tion
Wired as DTE Use 1:1 cable to MODEM
WideAreaFlashe rBoard
Verticle Entry Shrow ded header
For bypassing the EPC2, j umper center to bridging position, pin 1 to pin 2. To put EPC2 into circuit, jumper pini to pin3, and pin2 t o pin 4.
If it is found t hat the configuration is correct, JU11, and JU12 can be installed during man ufacture.
nCE = pull- down
nCEO = open ckt
TRST = pul l-up
TDI = pu ll-up
TDO = pull-up
TMS = pull-up
TCK = pul l-up
nSTATUS = pu ll-up
CONFIG_DONE = pull-up
nCONFIG = pu ll-up
CPU-CLK is a clock that HAS to be t here at power up. FPGA-CLK must be delivered to the F PGA after the FPGA is configured (a documented work-a round) or a late version of Quartus must be us ed to compile.
Might want to add some of these nets to the NC net.
Service Connec tor for the convenie nce of software progr ammers. Utilizes multif unction pins.
DO not mount PRC_JTAG connector
XC2C256_TQ144
EPXA1F672I2
EPC2
HEADER 2X2
HEADER 2
2-Pin Header
Open Ckt
Jumper
Soft Reset
SOFT_RESET
Digi-Key A90 45-ND
RJ45 AMP 555764-1
MAX3241CWI
EPC BYPASS
EPC INLINE
JTAG ROUTING
AMP 2510-6002UB
2mm pitch SMD HEADER 10X2
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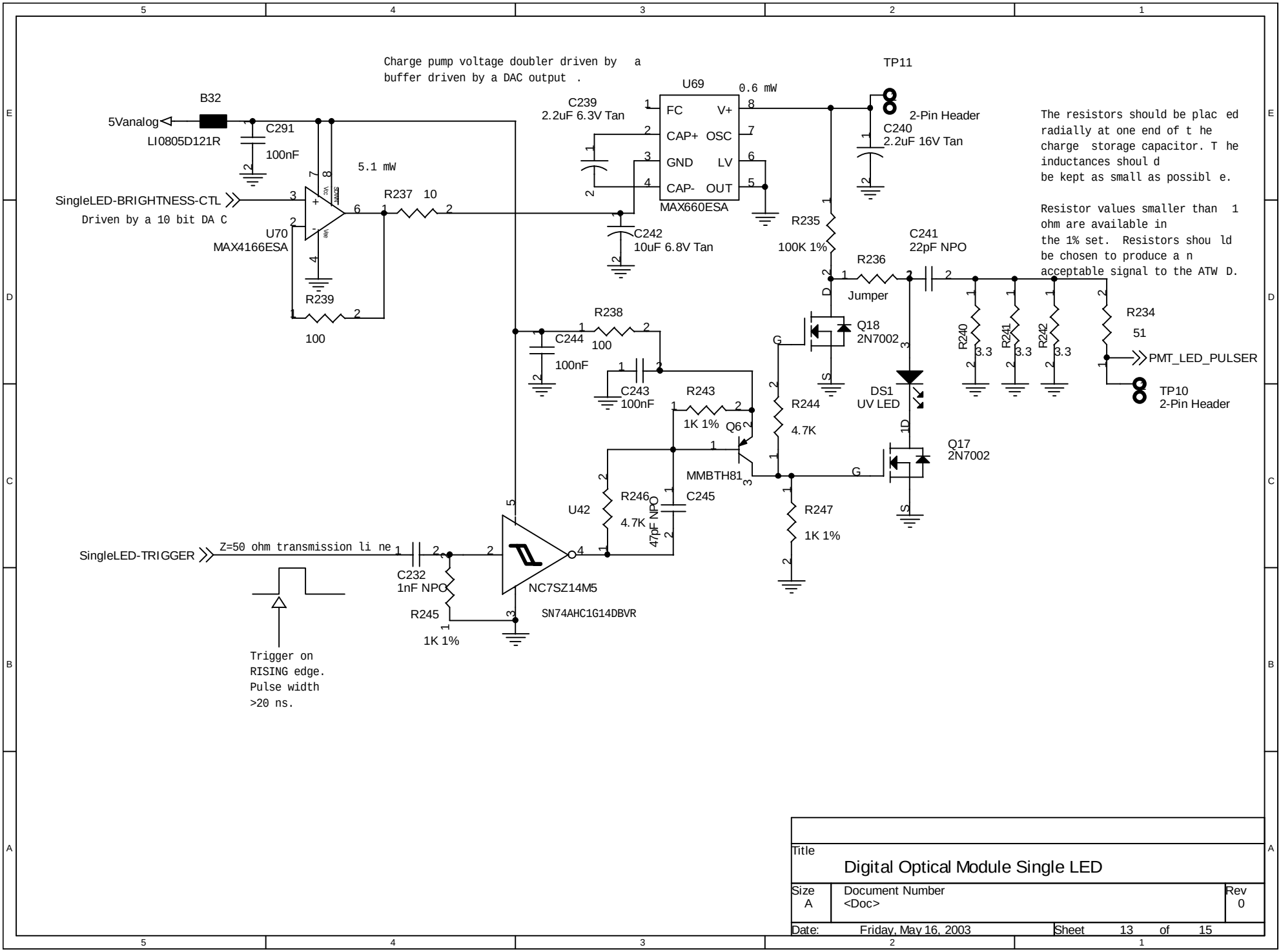

Title	Digital Optical Module Single LED	
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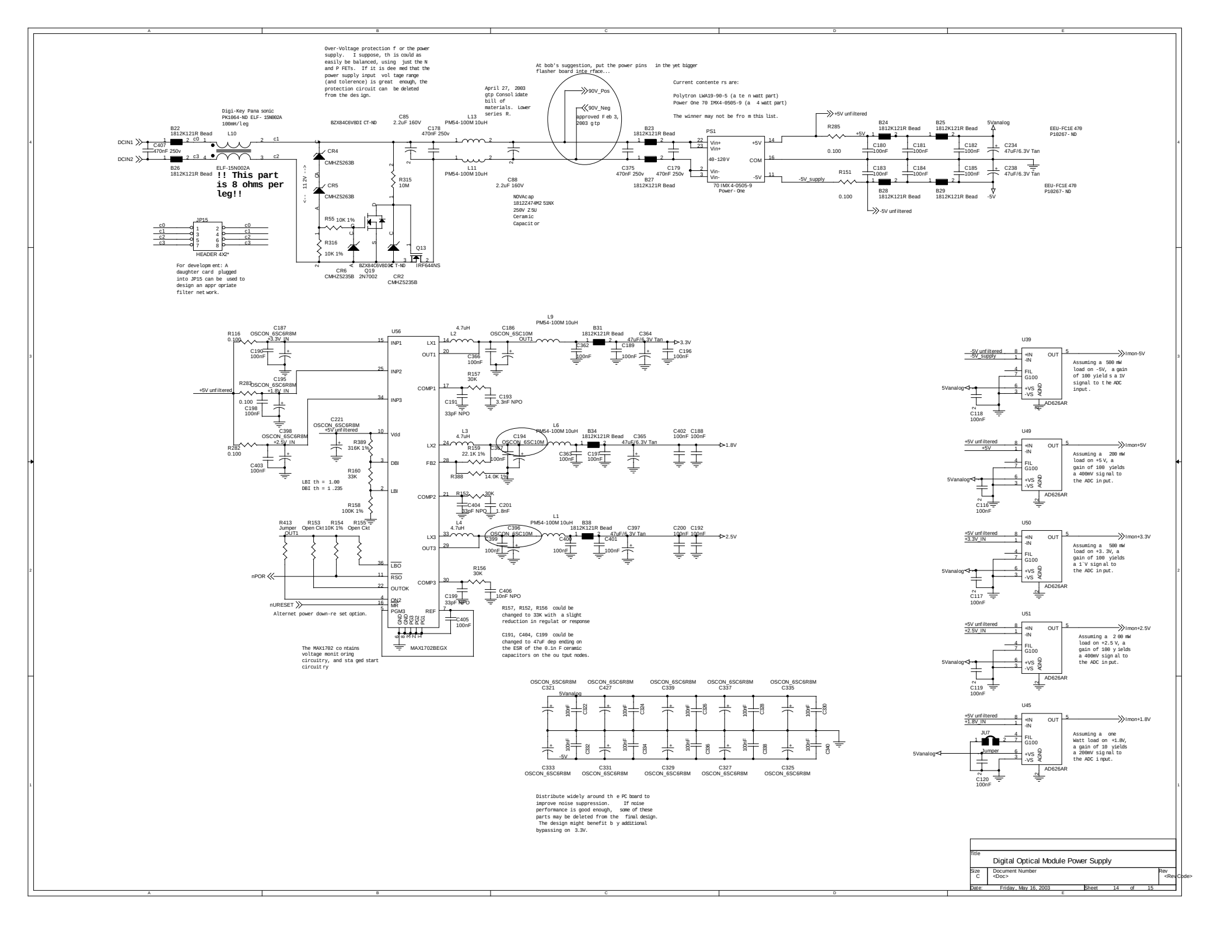
Over-Voltage protection f or the power supply. I suppose, th is could as easily be balanced, using just the N and P FETs. If it is dee med that the power supply input vol tage range (and tolerence) is great enough, the protection circuit can be deleted from the des ign.
At bob's suggestion, put the power pins in the yet bigger flasher board inte rface...
90V_Pos
90V_Neg
approved F eb 3, 2003 g tp
April 27, 2003 gtp Consol idate bill of materials. Lower series R.
Current contente rs are:
Polytron LWA19-90-5 (a te n watt part)
Power One 70 IMX4-0505-9 (a 4 watt part)
The winner may not be fro m this list.
Digi-Key Pana sonic PK1064-ND ELF- 15N002A 100mH/ Leg
DCIN1
DCIN2
C407 470nF 250v
B22 1812K121R Bead
B26 1812K121R Bead
L10
ELF-15N002A
!! This part is 8 ohms per leg!!
BZX84C6V8DI CT-ND
C85 2.2uF 160V
C178 470nF 250v
L13 PM54-100M 10uH
L11 PM54-100M 10uH
C88 2.2uF 160V
CR4 CMHZ5263B
CR5 CMHZ5263B
R315 10M
R55 10K 1%
R316 10K 1%
Q13 IRF644NS
CR6 CMHZ5235B
Q19 2N7002
BZX84C6V8DI CT-ND
CR2 CMHZ5235B
<-- 11.2V -->
NOVAcap 1812Z474M2 5INX 250V Z5U Ceramic Capacit or
B23 1812K121R Bead
B27 1812K121R Bead
C375 470nF 250v
C179 470nF 250v
PS1
70 IMX4-0505-9 Power- One
+5V unfiltered
-5V unfiltered
-5V_supply
R285 0.100
R151 0.100
B24 1812K121R Bead
B25 1812K121R Bead
B28 1812K121R Bead
B29 1812K121R Bead
5Vanalog
C180 100nF
C181 100nF
C182 100nF
C183 100nF
C184 100nF
C185 100nF
C234 47uF/6.3V Tan
C238 47uF/6.3V Tan
EEU-FC1E 470 P10267- ND
EEU-FC1E 470 P10267- ND
JP15
HEADER 4X2*
For developm ent: A daughter card plugged into JP15 can be used to design an appr opriate filter net work.
L9 PM54-100M 10uH
R116 0.100
C187 OSCON_6SC6R8M +3.3V IN
C190 100nF
C195 OSCON_6SC6R8M +1.8V IN
R283 0.100
C198 100nF
C398 OSCON_6SC6R8M +2.5V IN
R282 0.100
C403 100nF
C221 OSCON_6SC6R8M +5V unfiltered
R389 316K 1%
R160 33K
R158 100K 1%
LBI th = 1.00
DBI th = 1.235
U56
MAX1702BEGX
INP1
INP2
INP3
Vdd
DBI
LBI
LBO
RSO
OUTOK
ON2
MR
PGM3
REF
LX1
OUT1
COMP1
LX2
FB2
COMP2
LX3
OUT3
COMP3
L2 4.7uH
C186 OSCON_6SC10M OUT1
B31 1812K121R Bead
C362 100nF
C189 100nF
C364 47uF/6.3V Tan
C196 100nF
3.3V
C366 100nF
R157 30K
C191 33pF NPO
C193 3.3nF NPO
L3 4.7uH
C194 OSCON_6SC10M
L6 PM54-100M 10uH
B34 1812K121R Bead
C365 47uF/6.3V Tan
C402 100nF
C188 100nF
1.8V
C367 100nF
R159 22.1K 1%
R388 14.0K 1%
C363 100nF
C197 100nF
R152 30K
C404 33pF NPO
C201 1.8nF
L4 4.7uH
C396 OSCON_6SC10M
L1 PM54-100M 10uH
B38 1812K121R Bead
C397 47uF/6.3V Tan
C200 100nF
C192 100nF
2.5V
C399 100nF
C401 100nF
C401 100nF
R156 30K
C406 10nF NPO
C199 33pF NPO
C405 100nF
R413 Jumper OUT1
R153 Open Ckt
R154 10K 1%
R155 Open Ckt
nPOR
nURESET
Alternet power down-re set option.
The MAX1702 co ntains voltage monit oring circuitry, and sta ged start circuit ry
R157, R152, R156 could be changed to 33K with a slight reduction in regulat or response
C191, C404, C199 could be changed to 47uF dep ending on the ESR of the 0.1in F ceramic capacitors on the ou tput nodes.
OSCON_6SC6R8M C321
OSCON_6SC6R8M C427
OSCON_6SC6R8M C339
OSCON_6SC6R8M C337
OSCON_6SC6R8M C335
5Vanalog
-5V
C333 OSCON_6SC6R8M
C331 OSCON_6SC6R8M
C329 OSCON_6SC6R8M
C327 OSCON_6SC6R8M
C325 OSCON_6SC6R8M
Distribute widely around th e PC board to improve noise suppression. If noise performance is good enough, some of these parts may be deleted from the final design. The design might benefit b y additional bypassing on 3.3V.
U39
-5V unfiltered
-5V_supply
5Vanalog
Imon-5V
Assuming a 500 mW load on -5V, a gain of 100 yield s a 1V signal to t he ADC input .
AD626AR
C118 100nF
U49
+5V unfiltered
+5V
Imon+5V
Assuming a 200 mW load on +5 V, a gain of 100 yields a 400mV sig nal to the ADC in put.
C116 100nF
U50
+5V unfiltered
+3.3V IN
Imon+3.3V
Assuming a 500 mW load on +3. 3V, a gain of 100 yields a 1 V sign al to the ADC in put.
C117 100nF
U51
+5V unfiltered
+2.5V IN
Imon+2.5V
Assuming a 2 80 mW load on +2.5 V, a gain of 100 y ields a 400mV sign al to the ADC in put.
C119 100nF
U45
+5V unfiltered
+1.8V IN
Imon+1.8V
JU7
Jumper
Assuming a one Watt load on +1.8V, a gain of 10 yields a 200mV sig nal to the ADC i nput.
C120 100nF
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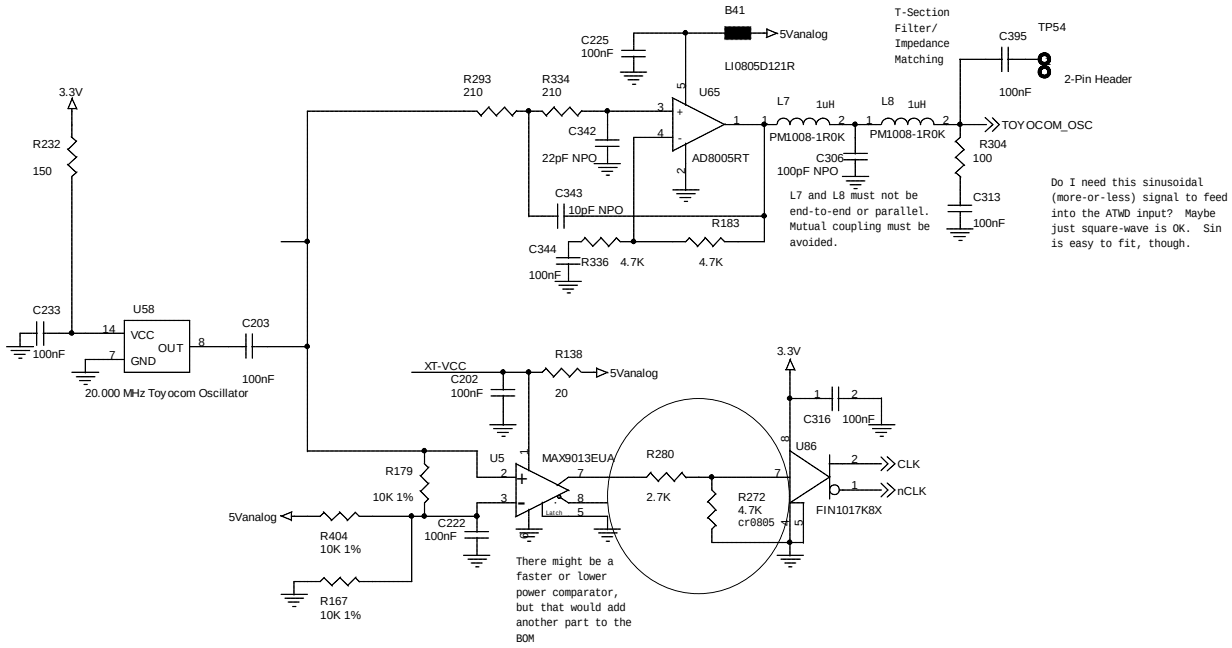

Title	Digital Optical Module Crystal	
Size B	Document Number <Doc>	Rev <Rev Code>
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