Board Stack-up:
TOP- Routing- Flud with ground plane where possible
Prepreg
INNER1 - Routing - controlled impedance pairs and general routing
Prepreg
GND - Power Plane
0.004" Prepreg
3.3V - Power Plane
Prepreg
INNER2 - Controlled Impedance and general routing
Prepreg
BOTTOM- Routing- Flood with copper where possible

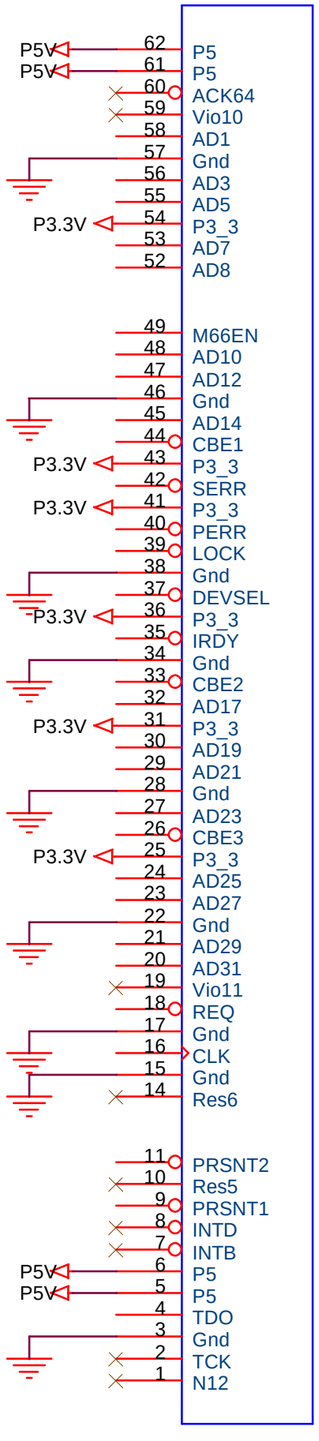
Layout:
"Front" refers to the edge of the board to the right when looking at the component side of the board with PCI connector down.
Lay out LVDS pairs according to recommendations in Ch. 4 of http://www.national.com/appinfo/lvds/files/LOM_2.pdf.
Locate comparators and logic near front panel.
Locate DB-9 and LEMO connectors near each other.
Locate test connector at top (as close to top as reasonable),
Locate harmonica connector at back of board with openings facing up.
Space harmonica connector at least 1/2" down from top edge of board to allow for cable routing inside computer.
Locate LVDS drivers near harmonica connector.
MAKE LVDS PAIRS BETWEEN DRIVER AND HARMONICA CONNECTOR ALL THE SAME LENGTH!!!
Match lengths of + and - LVDS lines in pairs. (see reference)
Jumper footprints and open-ckt footprints should be the same size to permit easy configuration change.

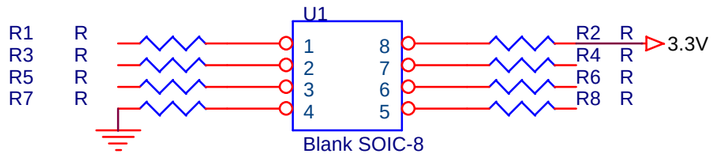
Build:
Both Y1 and Y2 cannot be mounted at the same time.

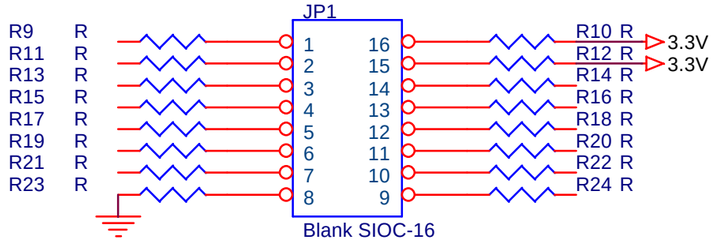
Rev B Changes
1) change R63 to open circuit, Change C40 (from JP3 to U13-2) to R119 = 4.7K.
2) R66 & R68 pads to 1210 size.
3) Suggest change 1uF Capacitors, C18, C23, C24, C27, C36, C38, C44, C45, C50, C58, C61, C63, C65, C67, C68, C72 and C74, to X7R Ceramic (DC020703FIF) 0805 size
4) R26, R27, R32 to 511ohm 0805.
5) S1 connect only to pin 1, pin2, the switch contacts.
6) Change regulator, U2, to National Semiconductor LP3964 EMP-3.3
7) Add fuses F1, F2, F3
8) Add provisional loading instructions to build instructions to loading house.
9) Change Y1 footprint. Three of 5 pads out of position.
10) Add four protective diodes, D9, D10, D11 and D12.
11) Add ground pins on JP3 (RJ45 input connector)
12) Add ground pins on JP2A and JP2B
13) Change DS1, DS2, DS3 to a three-in-one verticle LED unit DS1a,b,c.
14) Add feature for using modem control lines to generate sync pulse.
15) Revise end panel layout to accommodate LED change. Allow for access to S1 from rear panel.
16) Shorten board by 1/16" (?)

Gerald Przybylski
Lawrence Berkeley National Laboratory

Title: Fabrication (Rev B 7/7/04)		
Size: A	Document Number: DSB-Sheet1	Rev: A
Date: Thursday, August 05, 2004	Sheet 1 of 4	

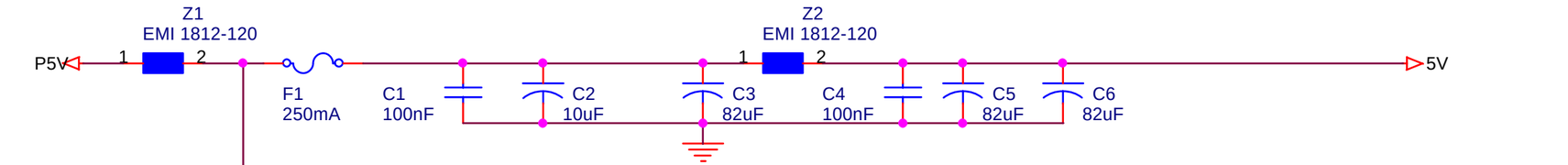


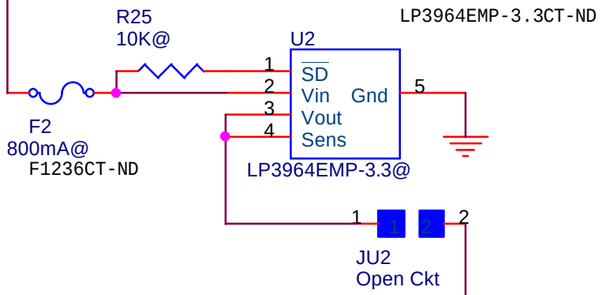




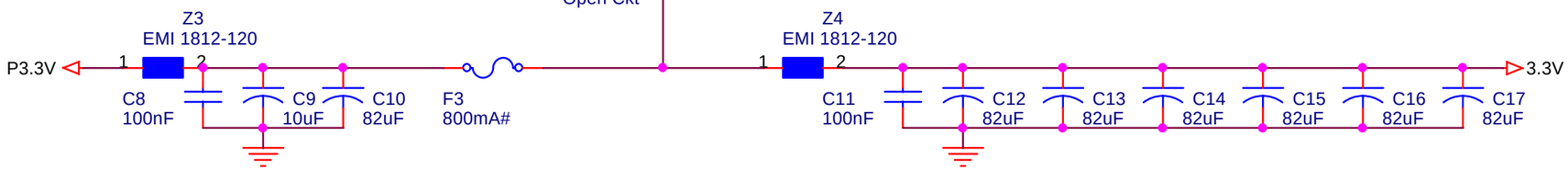
Uncommitted sockets for breadboarding, if required.

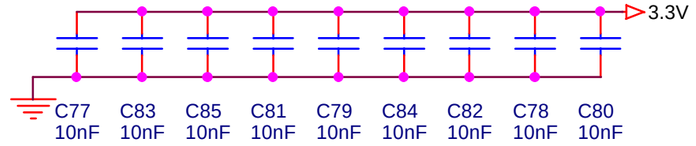
Title: Mechanical (Rev B 7/7/04)		
Size: A	Document Number: DSB-Sheet2	Rev: A
Date: Thursday, August 05, 2004	Sheet 2 of 4	



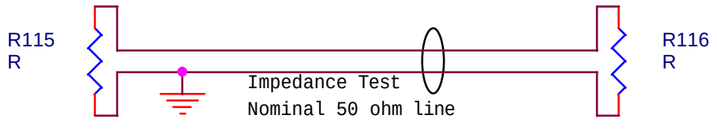


If 3.3V is not available from the
PCI bus mount U2 and JU1.





When the board will be used with
a 5V only computer, then mount
the components with values ending
in "@", and leave the components
ending in "#" out. Also,install
jumper JU2.
Normal configuraton is with F3
mounted, and U2 not mounted.



Gerald Przybylski
Lawrence Berkeley National Laboratory

Title: Power (Rev B 7/7/04)		
Size: A	Document Number: DSB-Sheet 3	Rev: A
Date: Thursday, August 05, 2004	Sheet 3 of 4	

size0805
R26 511
R27 511
R30 5.6K
R31 5.6K
DS1B
DS1C
350-1274-ND
tripple LED module
http://rocky.digikey.com/WebLib/Dialight/Web%20Data/564-0x00-xxx.pdf
564-0100-111 LED Digi-Key 350-1274-ND
GPS_DET
MC_DET
Q2 MMBT2222A/SOT
Q3 MMBT2222A/SOT
R28 1K
R29 5.6K
Q1 MMBT2907A/SOT
~4.9V when INTERNAL is true
C21 100nF
C23 1uF
U4 ADR423AR
TP Vin NC NC Vout Gnd Trim
C22 100nF
MC_DET
GPS_DET
EXTERNAL
U6 SN74AHCT1G32DCK
R117 1.8K
R118 3.3K
DS1A
564-0100-111 LED Digi-Key 350-1274-ND
R32 511
size0805
C25 100nF
C30 100nF
3.000V
Y1 Corning C2560 20.000MHz Osc.
Vdd NC GND Out GND
C28 100nF
D2 MMBD4148
D1 MMBD4148
R42 2K
C31 100nF
C32 10uF
Y2 20.000 MHz Toyocom Oscillator*
VCC OUT GND
10.000MHz Toyocom Oscillator optional
C24 1uF
C26 10nF
R40 11K
R41 100
R48 5.11K
U7 LT1711CMS
R45 Oper Ckt
R47 Oper Ckt
R46 511
C27 1uF
C29 10nF
INTERNAL
U8 DS90LV001TM
R44 100
C34 100nF
R51 100
R53 Jumper
R52 Open Ckt
INT_CLK
R49 Jumper
R54 Jumper
U10A SN74AHC74D
R56 100
TP1 2-Pin x 0.100" Header (no-load)
R_DATA
MC_SER+
MC_SER-
R36 100
R38 100
U5 SN75175D
R34 100
R35 100
R33 1K
R37 10K
R39 10K
R43 10K
U3 DS90LV110TMTC
SER1+ SER1- SER0+ SER0- SER_TP+ SER_TP- SER7+ SER7- SER6+ SER6- SER5+ SER5- SER4+ SER4- SER3+ SER3- SER2+ SER2-
C18 1uF
C19 100nF
C33 100nF
INTERNAL
INT_PGM_PULSE
R50 100
U9 SN74AHC1G126DCK
TP2 2-Pin x 0.100" Header (no-load)
C36 1uF
C35 100nF
U11 DS90LV110TMTC
PPS1+ PPS1- PPS0+ PPS0- PPS_TP+ PPS_TP- PPS7+ PPS7- PPS6+ PPS6- PPS5+ PPS5- PPS4+ PPS4- PPS3+ PPS3- PPS2+ PPS2-
C37 100nF
GPS_PPS
U12
R55 1K
R57 100
SN74AHC1G126DCK
R58 10K
R61 10K
R62 10K
C41 100nF
MC_PPS
R65 100
U14 SN74AHC1G126DCK
C47 100nF
U15 SN74AHC1G08DCK
INT_PGM_PULSE
C51 100nF
C55 100nF
R73 1K
R75 Open Ckt
Front Panel Switch
C&K KT11BxSAM
S1, any of C&K KT11B0SAM KT11B1SAM KT11B2SAM KT11P3SA1M KT11P4SA1M
Pin 1 and 2 are the inner pins.
Pin 3 and 4 are frame.
S1
R78 Jumper
R76 Open Ckt
INT_CLK
R113 100
R114 100
U18A SN74AHC74D
U18B SN74AHC74D
R70 100
R72 100
R79 100
R80 100
C50 1uF
JP2 8-8RJ-45x8
SER0+ SER0- PPS0+ PPS0- CLK0+ CLK0-
SER1+ SER1- PPS1+ PPS1- CLK1+ CLK1-
SER2+ SER2- PPS2+ PPS2- CLK2+ CLK2-
SER3+ SER3- PPS3+ PPS3- CLK3+ CLK3-
SER4+ SER4- PPS4+ PPS4- CLK4+ CLK4-
SER5+ SER5- PPS5+ PPS5- CLK5+ CLK5-
SER6+ SER6- PPS6+ PPS6- CLK6+ CLK6-
SER7+ SER7- PPS7+ PPS7- CLK7+ CLK7-
Socket candidates are Molex 44248-0060 44248-0064 44248-0113 44248-0114 top-release ganged RJ-45 socket, unshielded..
C57 100nF
R82 100
R83 100
R84 100
U10B SN74AHC74D
R88 100
Spare
RS-232 DTE
J2 CON_SUBD-9-Male
CS
R_Data
DR
Front Panel Jack
1PPS input to LEMO may be 50% duty cycle
J3 EPL.00.250.DTA
J4 EPL.00.250.DTA
R66 51 R1210
R68 51 R1210
5mm Lemo Right Angle PCB connector
D9 MMBD4148
D10 MMBD4148
R119 4.7K
R59 11K
R60 11K
C38 1uF
C39 10nF
R63 Open Ckt
D3 MMBD4148
D4 MMBD4148
R64 5.11K
C42 100nF
C43 10uF
U13 LT1711CMS
C44 1uF
C46 10nF
D5 MMBD4148
D6 MMBD4148
C48 100nF
R69 2K
R67 11K
C52 100nF
C53 10uF
R74 5.11K
U16 LT1711CMS
C45 1uF
C49 10nF
R71 511
U17 DS90LV001TM
R77 100
C54 100nF
D7 BAS70-06/SOT
U19 SN74AHC1G125DCK
R81 5.11K
C56 100nF
All 1uF capacitors May be 0805 Ceramic X7R (Ask Jimmie Johnson)
DR
CS
R120 4.7K
R122 4.7K*
C86 100pF
C87 100nF
R121 11K
D13 MMBD4148
D14 MMBD4148
U28 SN74AHC1G125DCK
D11 MMBD4148
D12 MMBD4148
R94 1K
R101 100
U22 DS90LV110TMTC
CLK1+ CLK1- CLK0+ CLK0- CLK_TP+ CLK_TP- CLK7+ CLK7- CLK6+ CLK6- CLK5+ CLK5- CLK4+ CLK4- CLK3+ CLK3- CLK2+ CLK2-
C63 1uF
C64 100nF
SER_TP+
SER_TP-
R91 100
U21 DS90LVDS018ATM
R90 51
C61 1uF
C62 10nF
PPS_TP+
PPS_TP-
R99 100
U24 DS90LVDS018ATM
R96 51
C68 1uF
C69 10nF
CLK_TP+
CLK_TP-
R107 100
U27 DS90LVDS018ATM
R106 51
C74 1uF
C75 10nF
Rear Panel Test Port
0.100" RA Header S2122-10-ND
JP4
Ehternet Transformer for 10/100-Base-T
Pulse Engineering 1:1 turns ratio
PE-69012
T1
JP3 RJ-45
Front Panel Jack
1PPS input to RJ45 must be <1% duty cycle.
P+ P- CK+ CK-
MC_SER+
MC_SER-
R89 100
C60 100nF
R85 11K
R86 11K
C58 1uF
C59 10nF
R87 100
R92 4.75K
R93 5.11K
U20 LT1711CMS
R100 100
C71 100nF
R102 2K
R97 11K
C67 1uF
C70 10nF
R98 100
R105 5.11K
U25 LT1711CMS
R95 511
C65 1uF
C66 10nF
U23 DS90LV001TM
R104 100
C72 1uF
C73 10nF
R103 100
D8 BAS70-06/SOT
U26 SN74AHC1G126DCK
R108 5.11K
C76 100nF
Vcm=+1V is optimum. 10mV stabalization bias with no signal.
Controlled impedance pair. NO STUBS. Termination on each end.
Gerald Przybylski
Lawrence Berkeley National Laboratory
Title: Main Signal Processing (Rev B 7/7/04)
Size C | Document Number DSB-Sheet4 | Rev A
Date: Thursday, August 05, 2004 | Sheet 4 of 4